LONDON'S GLOBAL UNIVERSITY

Organic Semiconductors-Based Devices Electrical Reliability to Environmental Stress

Luca Santarelli

A dissertation submitted for the degree of Doctor of Philosophy

Department of Physics and Astronomy and London Centre for Nanotechnology

University College London

London, July 2017

I, Luca Santarelli, confirm that the work presented in this thesis is my own. Where information has been derived from other sources and work which has formed part of jointly authored publications has been used I confirm that this has been indicated in the thesis.

Supervisor: Prof. Franco Cacialli,
Department of Physics and Astronomy and London Centre for Nanotechnology,
University College London
Second Supervisor: Dr. Laurent Bozec
Eastman Dental Institute,
University College London

to my wife Lucia

to my family

Acknowledgments

My research was funded by the European Commission Seventh Framework Program (FP7/2007-2013) Marie Curie Initial Training Network under Grant Agreement No. 317488, (CONTEST).

A special thank goes to my supervisor Prof. Franco Cacialli who gave me the opportunity to be part of his team and who inspired my work.

I also express my gratitude to Dr. Laurent Bozec, my secondary supervisor, for his valuable support.

Great thanks go to Dr. Lim Tekfouy, Dr. Horst Gieser and Dr. Heinrich Wolf for hosting me in their group in Fraunhofer in Munich; to Dr. Vincenzo Vinciguerra for the time I spent in STMicroelectronics Catania; to Prof. Lugli and Engin Çagatay for the time I spent in their group at TUM.

I would thank CONTEST project coordinators Dr. R.S.Dahiya and Dr. Lorenzelli, project manager Elisa Morganti, fellows Simone Colasanti, Nagarajan Palavesam, Carlo Bagnato, Matjaž Ogrinc, Saleem Khan and all other people involved within CONTEST.

Finally, I would like to warmly thank Valentina Robbiano, Giuseppe Paternò, Andrea Zampetti, Alessandro Minotto, Ludovica Intilla, Francesco Bausi, Giulia Tregnago, Giovanni Francesco Cotella, Giuseppe Carnicella, Tecla Arcidiacono, Alexandros Rapidis, Keith Fraser and all other people who have been part of Prof. Cacialli's group with me, you've been so important to me.

Last, but not the least, I greatly thank my family, my friends and my wife Lucia for the support, love and encouragement they have always been giving to me.

Abstract

In this thesis, I report on the characterisation of the response of organic semiconductor based devices, namely organic light-emitting diodes (OLEDs), organic field-effect transistors (OFETs) and organic photovoltaic diodes (OPVDs) to environmental stress factors such as electrostatic discharge (ESD) and neutrons irradiation. The ESD stress was obtained by means of a transmission line-pulsing (TLP), responsible to generate current pulses with an increasing amplitude and a duration of few tens of nanoseconds. The exposure to neutron irradiation was obtained in the pulsed neutron and muon source at ISIS part of the Rutherford Appleton Laboratories (RAL). The tested devices were: P3HT (poly(3-hexylthiophene)):PCBM ([6,6]- phenyl C61 butyric acid methyl ester) bulk heterojunction solar cells; PBTTT (poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2- b]thiophene) and P3HT OFETs; F8BT (poly(9,9'-dioctylfluorene-alt-benzothiadiazole)) OLEDs. An analysis of both electrical (IV and JV curves, Electroluminescence (EL)) and optical (photoluminescence (PL), Raman Spectroscopy) characteristics of tested devices prior and following the exposure to various degrees of ESD, neutron irradiation or both is reported. For each tested device I obtained the respective TLP parameters (the leakage current (I_{LEAK}), the TLP current (I_{TLP}), the TLP voltage (V_{TLP}), the TLP resistance (R_{TLP})) and the correlation of these with parameters extracted by means of their electrical/optical characterisation, namely: (i) the charge mobility, the threshold voltage (V_{TH}) and the on/off ratio of OFETs; (ii) the current density (J_{sc}), the open-circuit voltage (V_{oc}), the fill factor (FF) and the power conversion efficiency (η) of OPVs; (iii) the turn-on voltage (V_{on}), the external quantum efficiency (EQE) and the EL maximum wavelength emission (λ_{max}) of OLEDs.

Importantly, the activity carried out in this thesis gives novel insights about the response of conjugated polymer-based devices with respect to the stressing stimuli (ESD events, cosmic rays) they are exposed to in their most suitable application fields (space, medicine, robotics), such as the energy necessary to cause a total or partial failure during ESD events, the requirements necessary to design electrical protections, the expected loss of device figures after a decade of exposure to cosmic rays. Interestingly, the results in this thesis reported point out, in most of the cases, an excellent robustness of these devices to both ESD and cosmic rays stress. In fact, whilst technology silicon-based is found to suffer a permanent failure in most of the cases for an applied TLP power lower than 400 W, polymer-based technology was found to withstand up to 800 W (OPVs and OLEDs) without suffering permanent damages. As regards the stress correlated to the same dose of

neutrons irradiation, optoelectronic devices based on inorganic semiconductors suffer of a 90% reduction of their figures of merit (J_{SC}, η), whilst the same figures are reduced of only 20% in polymer-based devices.

Although previous works are reported in literature, the work reported in this thesis, at the best of my knowledge, is the first work reporting a systematic quantitative TLP characterisation of organic devices along with a qualitative description of the effects on the organic materials within these devices because of the conditions imposed by the TLP test (high-frequency, high-voltage). Therefore, this thesis opens a new scenario proposing an investigating tool aimed both at measuring parameters useful for the design of the devices and at highlighting organic materials properties that can lead organic electronics to gain its definitive momentum.

Contents

List of Figures

List of Tables

List of Publications

Publications containing work also reported in this thesis:

- Santarelli, L.; Lim, T.; Wolf, H.; Gieser, H. and Cacialli, F. (2015); "*The Resilience of P3HT Field-Effect Transistors with respect to ESD Effects"*, 14. ESD-FORUM, 2015, pp. 67-76.
- Lim, T., Gieser, H., Santarelli, L., & Cacialli, F. (2015, June); *"Electrostatic discharge sensitivity investigation on organic field-effect thin film transistors".* New Circuits and Systems Conference (NEWCAS), 2015 IEEE 13th International (pp. 1-4). IEEE.

Publications in preparation and soon to be submitted:

- L. Santarelli, T. Lim, A. Minotto, A. Zampetti, H. Wolf, H. Gieser & F. Cacialli *"The Resilience of Bulk-Heterojunction Solar Cells with respect to Electrostatic Discharge Effects"***-in preparation**
- L. Santarelli, T. Lim, G. Paternò, A. Zampetti, H. Wolf, H. Gieser & F. Cacialli "*Electrostatic discharge effects over P3HT and PBTTT OFETs according different bias contexts*" **– in preparation**
- Giuseppe M. Paternò, Valentina Robbiano, Luca Santarelli, Andrea Zampetti, Christopher Frost, Victoria García Sakai and Franco Cacialli*. "In operando Neutron Radiation Damage Testing of Organic Solar Cells"* **– in preparation**
- L. Santarelli, T. Lim, G. Paternò, A. Zampetti, H. Wolf, H. Gieser & F. Cacialli "*Electrostatic discharge effects over neutron-hardened P3HT OFETs*" **– in preparation**

Other publications:

- Robbiano, V., Abdellah, A., Santarelli, L., Falco, A., El-Molla, S., Titova, L. V., & Lugli, P. "*Analysis of sprayed Carbon nanotube films on rigid and flexible substrates"* 2014 IEEE 14th International Conference in Nanotecnology (IEEE-NANO)

List of Abbreviations

BE	Binding energy
BHJ	Bulk heterojunction
CP	Conjugated polymer
DGneg	Negative pulses between the drain and the gate with the source left floating
DGpos	Positive pulses between the drain and the gate with the source left floating
DSneg	Negative pulses between the drain and the source with the gate grounded
DSneg-20$V_g$bias	Negative pulses between the drain and the source with a gate bias of -20 V
DSneg10$V_g$bias	Negative pulses between the drain and the source with a gate bias of 10 V
DSpos	Positive pulses between the drain and the source with the gate grounded
DSpos-20$V_g$bias	Positive pulses between the drain and the source with a gate bias of -20 V
DSpos10$V_g$bias	Positive pulses between the drain and the source with a gate bias of 10 V
DUT	Device under test
ECL	Electron-collection layer
EL	Electroluminescence
EQE	External quantum efficiency
ESD	Electrostatic discharge
ETL	Electron-transport layer
F8BT	Poly(9,9'-dioctylfluorene-alt-benzothiadiazole)
FF	Fill factor
HBM	Human body model
HCL	Hole-collection layer
HIL	Hole-injection layer
HMDS	Hexamethyldisilazane

HOMO	Highest occupied molecular orbital
ISS	International space station
ITO	Indium tin oxide
IV	Current vs voltage
JLV	Current density-luminance vs voltage
JV	Current density vs voltage
LED	Light-emitting diode
LUMO	Lowest unoccupied molecular orbital
OFET	Organic field-effect transistor
OLED	Organic light-emitting diode
OPV	Organic photovoltaic
OPVD	Organic photovoltaic diode
P3HT	Poly(3-hexylthiophene-2,5-diyl)
PBTTT	Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2- b]thiophene
PCBM	[6,6]- Phenyl C61 butyric acid methyl ester
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate)
PL	Photoluminescence
PTFE	Polytetrafluoroethylene
rpm	Rounds per minute
RT	Room temperature
SMU	Source measurement unit
TCO	Transparent conductive oxide
TFT	Thin films transistor
TLP	Transmission line-pulsing

List of Symbols

E_{TR}	Trigger energy
I_{DSMAX}	Maximum amplitude of the drain-source current
I_{LEAK}	Leakage Current
I_{ST}	Sub-threshold current
I_{TLP}	Transmission line-pulsing current
I_{TR}	Trigger current
J_{sc}	Short-circuit current density
Max-L	Maximum luminance
On/off	On off current ratio
P_{TLP}	Transmission line-pulsing power
P_{TR}	Trigger power
R_S	Series resistance
R_{SH}	Shunt resistance
R_{TLP}	Transmission line-pulsing resistance
R_{TLP}	Transmission line-pulsing resistance
V_{AC}	Anode-cathode voltage
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_{HV}	Voltage generated by the pulse generator
V_{inc}	Pre-charge voltage
V_{oc}	Open circuit voltage
V_{ref}	Voltage reflected by the DUT
V_{TH}	Threshold Voltage

V_{TLP}	Transmission line-pulsing voltage
V_{TR}	Trigger voltage
μ	Field-effect charge carrier mobility
η	Power conversion efficiency
λ_{max}	EL maximum wavelength emission

Introduction

Conjugated polymers (CPs) have been captivating attention since their discovery, back in 1977. Undoubtedly, one of the major breakthrough came thanks to the finding of the possibility of doping conjugated polymers[1], [2], and thus indicating, among all the possible applications, a particular suitability as active materials in light-emitting diodes (LEDs), thin films transistors (TFT) and photovoltaic diodes (OPVs). Despite the relatively poor performances in comparison with inorganic based devices, many advantages arise thanks to CPs[3]–[6]. In fact, they can be processed using inexpensive and large-area scalable solution-based processes and integrated in flexible and lightweight devices[7], [8]. Importantly, lightweight and flexibility are highly desirable in wearable electronics, foldable-conformable sensors for medicine purposes, robotics, space and avionics[9]–[13]. Despite such appealing properties, a large deployment of CPs devices also depends on the development of reliable systems based on them, able to sustain in the long-term the stress they undergo because of the environment they operate in. For instance, especially wearable devices, and more generally all electronic devices handled by users who could inadvertently act as short-circuit to such devices, can be interested by electrostatic discharge (ESD) phenomena. In fact, in inorganic electronic circuits the characterisation of the response to ESD phenomena and the design of protections are well established procedures since, if interested, devices can easily be destroyed by such events[14]–[16]. Surprisingly, the characterisation of organic devices with respect to ESD events has received little attention so far in the literature. Besides ESD events, another damaging stress source for electronic devices used for aircraft or spacecraft purposes is cosmic rays and neutrons irradiation. In fact, secondary neutrons are produced because of interaction of cosmic rays with either atmosphere or shielding layer of planes and spaceships. Upon exposure to such particles, electronic circuits can result temporarily or permanently affected since neutrons interact with nuclei of the atoms composing circuit elements[17]. To prevent total device failure redundant circuitry can be designed to replace damaged one and lower total failure likelihood[18], [19]. Nevertheless, all equipment, and crew too, are exposed to neutrons irradiation, therefore the characterisation of long-term effects on devices of neutrons hardening, within neutron sources facilities, is an important investigation technique for instruments to be employed in such environments[20], [21].

Aims of the work

In this thesis, I present the results about: i) the characterisation of the response to ESD phenomena of P3HT (Poly(3-hexylthiophene-2,5-diyl)) and PBTTT (Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene)) OFETs, of P3HT:PCBM ([6,6]-Phenyl-C61-butyric acid methyl ester) bulk heterojunction OPVs and of F8BT (Poly(9,9-dioctylfluorene-alt-benzothiadiazole)) OLEDs; ii) the neutron hardening of P3HT OFETs and P3HT:PCBM OPVs. Although many works related on the characterisation of aforementioned devices can be found in literature, the research activity in this thesis reported establishes a novel characterisation approach for these.

Importantly, I observed that the response to ESD phenomena changes according to the working condition of the devices. For instance, the response to ESD phenomena of an OFET working in the saturation regime is different from the response of the same OFET tested in correspondence of "off" state condition (gate-closed). Analogously, OPVs show different ESD responses in illumination conditions respect to dark conditions. Also, OLEDs show different ESD resiliency in "on" state conditions in comparison to "off" state conditions. Therefore, an accurate characterisation needs to be carried out per each of the possible working regimes of a device. Such characterisation was obtained by means of a transmission line-pulsing (TLP) system, an investigation tool that reproduces on workbench ESD-like pulses of duration approximately of 100 ns and configurable amplitude. Such characterisation gives important insights into OFETs, OPVs and OLEDs behaviour during ESD events such as the maximum current they can sustain before occurring into a failure, the overall conductance electrostatic discharge encounter by flowing through the devices and, not less importantly, the parasitic phenomena taking place in these devices because of the high-frequency domain (GHz) they are forced to work. The work carried out regarding TLP characterisation of P3HT and PBTTT OFETs are among the first reported works on TLP-stressed TFTs, and to the best of my knowledge, the only ones involving these two materials. Furthermore, no works about TLP characterisation of OPVs or OLEDs have been reported so far.

Cosmic rays, composed by protons and atomic nuclei, affect devices meant to be used in space and avionics applications. Neutrons irradiation provides a stressing environment useful for the simulation of the effects of cosmic rays on electronic devices. In such regard, I report in this thesis the result I obtained about "in operando OPVs" irradiated with neutrons of which the functionality, and the related photovoltaics parameters, were measured every 15 minutes throughout the irradiation period. Such tests revealed an unexpected robustness of P3HT:PCBM devices since their

photovoltaics parameters are only slightly degraded after an exposure dose equivalent to a decade exposure on the International Space Station (ISS). I also analysed neutron-exposed P3HT OFETs response to ESD phenomena, to assess the combination of both stress kinds on instruments employing organic transistors for space application. The combination of both stresses resulted particularly damaging for polymer crystal domains and for the molecular order/aggregation of the CPs used in these devices. The work in this dissertation reported about neutron radiation hardening of electronic devices based on CPs is part of a much larger investigation lead by Dr. Paternò, Dr. Sakai and Prof. Cacialli that, to the best of my knowledge, has been producing the very first papers reported on such topic so far[10], [22].

The results reported in this thesis are valuable for the development of ad hoc designed ESD protections for organic devices and for the understanding of OPVs and OFETs neutrons hardened behaviour. The first outcome paves the route to a larger deployment of CPs based devices whilst the second one underlines a further advantage in the utilisation of OPVs since these show a great ability to withstand massive doses of neutron irradiation without a dramatic loss of their performances. Furthermore, the results in this thesis reported show how polymer-based devices are robust to both ESD and cosmic ray stress. Silicon-based technology is found to suffer permanent failure, in the best cases, for an applied TLP power of 400 W[15], [23], whilst polymer-based technology was found to withstand up to 800 W (OPVs and OLEDs) without suffering of damages. As regards the stress correlated to the same dose of neutrons irradiation, optoelectronic devices based on inorganic semiconductors suffer of a ~90% reduction of their figures of merit (J_{SC}, η) [24], whilst in polymer-based devices the same figures are reduced up to ~20%.

Overview of the thesis

In **chapter 1**, I introduce all main concepts concerning CPs, OFETs, OPVs, OLEDs, TLP and neutron radiation hardening tests. About CPs, the properties arising in these because of carbon atoms sp^2 hybridisation, leading to the formation of HOMO and LUMO bands, are described. Furthermore, I describe how electric charges transport within the polymers are depending mostly on the dielectric constant of CPs, on the electrons-lattice coupling and on the structural disorder of CPs. Charge transport in CPs takes place via hopping between localised energy states, namely solitons and polarons. Upon photoexcitation or electric excitation, excitons are formed within CPs. These quasi-particles are fundamental in OPVs and OLEDs since the split of the hole from the electron within a formed exciton is the principle OPVs are based on, whereas their recombination is the one exploited

in OLEDs. Hence, in this chapter, a brief description of parameters characterising OPVs and OLEDs are introduced. Similarly, parameters characterising OFETs are described. The principles TLP test rely on are introduced and discussed so as to furnish a sufficient understanding of the analysis reported in the following chapters. Finally, an introduction on the fundamental principles neutrons irradiation technique is based on is reported.

Chapter 2 briefly introduces the materials used to carry on the research activity in this thesis reported, namely P3HT, PCBM, PBTTT and F8BT, as well as the fabrication processes of the devices (OPVs, OLEDs and OFETs) based on these materials. A description of the electrical, optical and TLP characterisation techniques used to analyse TLP stressed devices is reported. The last part of the chapter focuses on the neutron radiation hardening of OPVs and OFETs, describing the energy spectrum of neutrons used over these devices.

In **chapter 3** the results about the TLP characterisation of OPVs, OFETs and OLEDs are reported and discussed. Each kind of device was tested according different operation conditions so as to shed light on the ESD response in correspondence of different bias conditions of the active layer. Hence, TLP parameters are obtained out of each case-study. OPVs photovoltaics parameters were calculated before and after the TLP tests and the same procedure was followed to measure the electrical parameters of OLEDs and OFETs. Raman spectroscopy of PBTTT and P3HT OFETs and PL investigations of OPVs, carried out before and after the TLP tests, in this chapter are presented.

In **chapter 4**, the results obtained regarding OPVs neutrons hardened are reported. OPVs are irradiated in operando conditions, and devices parameters were calculated every 15 minutes throughout the irradiation period. Furthermore, in this chapter, the results obtained on TLP tested OFETs previously exposed to three different level of neutron doses are also reported, pointing out the combination of both stress kinds on polymer domains by means of Raman spectroscopy.

Finally, in **chapter 5** considerations about the whole research work carried out are presented.

1. Organic Optoelectronic Devices and Environmental Features

In this chapter, I introduce the main concepts regarding conjugated polymers electrical and optical properties. The functionality of OPVs, OFETs and OLEDs rely on such properties, hence the working principles and the parameters used to characterise these devices are described. The third section of the chapter describes TLP test basic principles and TLP parameters extraction and interpretation, whereas the last section briefly introduces concepts at the basis of neutron irradiations techniques.

1.1 Conjugated polymers

Polymers are material characterised by many repetitive structural units called monomers. In fact, the term polymer derives from *poly*, meaning many, and *mer*, meaning units. Therefore, a monomer is any unit that can generate a polymer by means of a process called *polymerisation* [25]–[27]. Polymers can be classified according different criteria, such as according to their chain chemistry (carbon-chain or heterochain polymers), to their macroscopic structure (linear, branched or crosslinked polymers) or according their formability (thermo-plastics or thermoset polymer)[28]–[30]. A proper description of the properties of the polymers belonging to each of these classes is by far beyond the purposes of this thesis. I will focus my attention only on a specific group of polymers, i.e. the semiconductive polymers.

Semiconductive polymers have been increasingly captivating attention since Shirakawa and McDiarmid discovered a way to significantly enhance the electrical conductivity in doped polyacetylene in 1977 [2]. The electrical, optical and mechanical properties[5], [31]–[33] (flexibility and lightweight) featured along with an easy and cheap processing render semiconductive polymers particularly suitable for optoelectronic devices such as *organic light-emitting diodes* (OLEDs)[34]–[38], *organic photovoltaic cells* (OPVs)[3], [39], [40] and *organic field-effect transistors* (OFETs)[41], [42]. Semiconductive polymers are encompassed in larger area of materials defined as organic semiconductors that comprises also small molecules. In semiconductive polymers, the carbon atoms exhibit sp^2 hybridization, due to a mixing of the 2s orbitals with two of the 3 available 2p orbitals, forming three sp^2 orbitals per each carbon, plus one free p orbital. Each carbon is therefore forming 3 coplanar bonds, defined σ bond and spatially distributed according an angle of 120°, with

the adjacent carbon atoms by means of the sp^2 hybrid orbitals. The remaining 2p orbital, which is not hybridized, is perpendicular to the sigma bond and it is defined as $2p_z$. When two $2p_z$ from two different carbon atoms are close enough to permit an overlap, a π orbital is formed, resulting in the creation of a double bond. The π bonds are weaker than σ ones because of a less overlap of the molecular orbitals. The semiconducting properties of these systems arise from the alternation of single (σ) and double bonds (σ + π) in the molecule and such system arrangement is called *conjugation*. Systems featuring conjugation are called *conjugated*, hence semiconductive polymers are more properly referred as *conjugated polymers* (CPs) (Figure 1-1). The simplest conjugated system is obtained from two carbon atoms hybridized sp^2 (ethene molecule $CH_2=CH_2$) in which the overlap of two $2p_z$ results in the formation of a molecular bond. Upon the rise of this molecular bond, two orbitals are formed, namely a bonding and an antibonding molecular orbital. The π orbital is lower in energy than the original $2p_z$ orbital, whereas the π* orbital is higher in energy than the original $2p_z$. Hence, the two electrons coming from the $2p_z$ original orbitals are energetically favoured to occupy the π orbital, in the ground state. The bonding orbital π is called the *highest occupied molecular orbital* (HOMO), whereas the anti-bonding orbital π* is called the *lowest unoccupied molecular orbital* (LUMO) (Figure 1-2). If we consider a larger number of sp^2 hybridized carbon atoms forming a conjugated system, for example trans-polyacetylene, the lateral overlap between π-orbitals permits the delocalisation of the π-electrons over the whole molecule so considerably reducing the HOMO-LUMO gap, and thus permitting the formation of quasi-continuous π (occupied) and π* (unoccupied) bands. Such delocalisation would lead polyacetylene to acts as a 1D metal with $2p_z$ electrons filling half of the π-band. If the real space periodicity of the chain is "a" and the 1D band is half filled the Fermi points are at ±π/a. However, such condition can be easily perturbed by elastic distortions causing a lowering of the symmetry and inducing so-called *Peierls distortions* [43], [44] or dimerization, which is energetically favoured and introducing a periodicity twice the original one (2a). A band gap at the Brillouin-zone boundaries ($k = \pm \pi/2a$) arises because of these new conditions and the overall electronic energy is lowered as filled electron states move below the new Fermi points ($\pm \pi/2a$), whereas empty states move above. As long as the strain energy introduced by the distortion does not match or exceeds the decrease of the electronic energy, the dimerization is favoured (Figure 1-3). According this mechanism, the trans-polyacetylene, and more generally the conjugated polymers, are characterised by an energy gap within the HOMO-LUMO. The optical band gap of undoped CPs is normally between 2 and 3 eV, while the electronic band gap is higher of ~ 0.5 – 1 eV of the latter due to the strong electron-hole

binding energy (~ 1 – 1.5 eV) [45]. The number of alternated single-double bonds in CPs, defined as *conjugation length*, affects the energy spacing between the HOMO and LUMO levels.

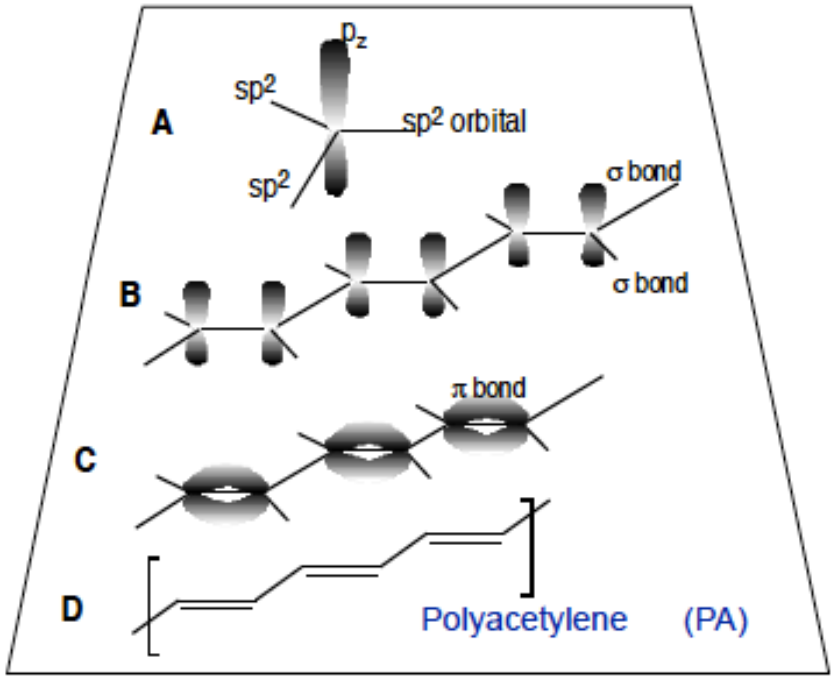


Figure 1-1: (a) Representation of the three hybridized sp^2 and the non-hybridized p_z orbitals. (b) The σ interaction between the hybridized sp^2 orbitals. (c) Alternate π-bonds in PA, originating from the lateral overlap between non-hybridised p_z orbitals. (d) The whole conjugated structure of trans-polyacetylene. Taken from[5].

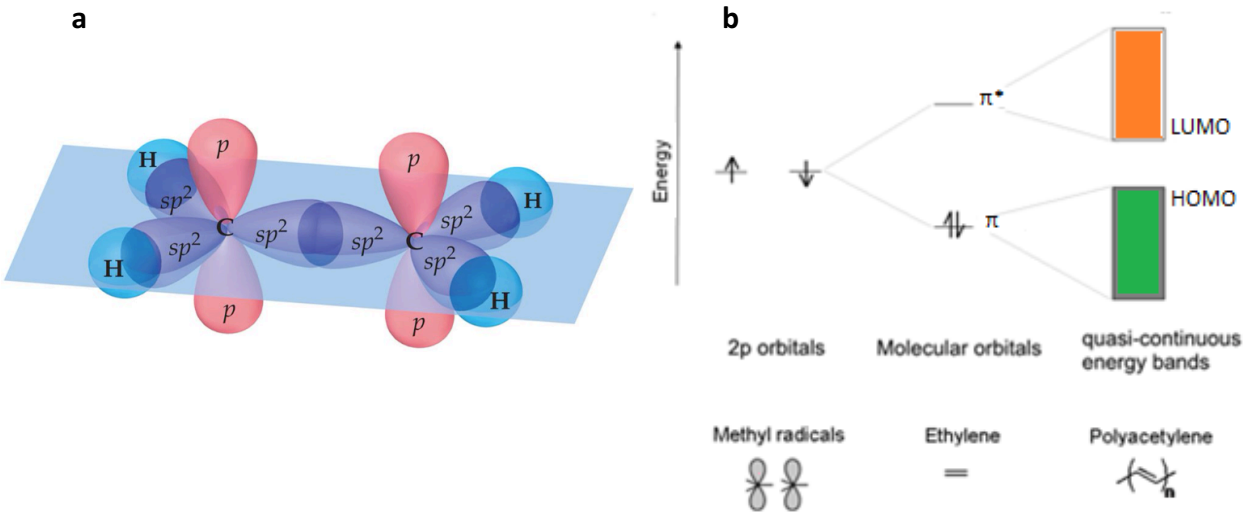


Figure 1-2: (a) Scheme of the sp^2 hybridization in an ethylene molecule. Taken from[46]. (b) Scheme of the energy splitting of $2p_z$ orbitals into a bonding and an antibonding orbital. From an increase of the CH_2 units, energy levels are lead into a degeneration resulting in two quasi-continuous bands, namely the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO).

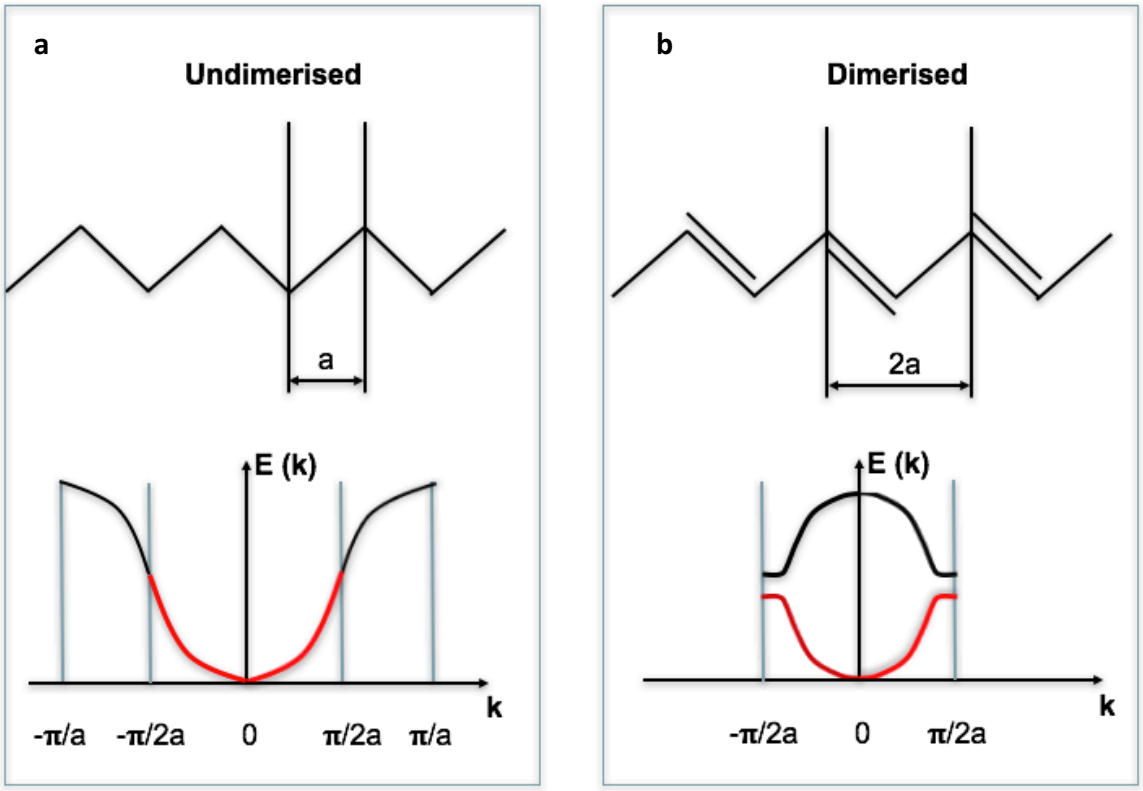


Figure 1-3: The effects of so-called Peierls distortions on the periodicity and the Fermi points of trans-polyacetylene, from an undimerised (metallic) form (a) to a dimerised one (b).

1.1.1 Solitons, polarons and excitations in CPs

CPs have been intensively studied as active layer of optoelectronic devices because of the localisation of electrical and photo-excitations they feature. Such property arises from mainly three synergistic effects taking place in CPs: i) the weak electron-electron screening due to the low dielectric constant (ε = 2 - 4) characterising CPs; ii) the electron-lattice coupling causing self-trapping of excited states and giving these a quasi-particle nature; iii) the broad and disordered density of electronic states caused by the structural disorder [47]. The charge transport in CPs greatly depends on these three phenomena. Upon chemical processes (i.e. oxidation/reduction) or electrical/photo treatments (charge injection/photo-oxidation) an excess of electric charge can be introduced in CPs, and, contrarily to what happens in conventional 3D semiconductors, these do not enter in the energetic bands of the polymers but induce kinks in the conjugated sequence. The consequences of these kinks depend whether the conjugated system possesses a doubly degenerated ground state or not. In those featuring a doubly degenerated ground state, such as trans-polyacetylene, introduced charges accommodate in defective states called *solitons* that behave as solitary localised waves in a range of 10-15 carbon atoms.

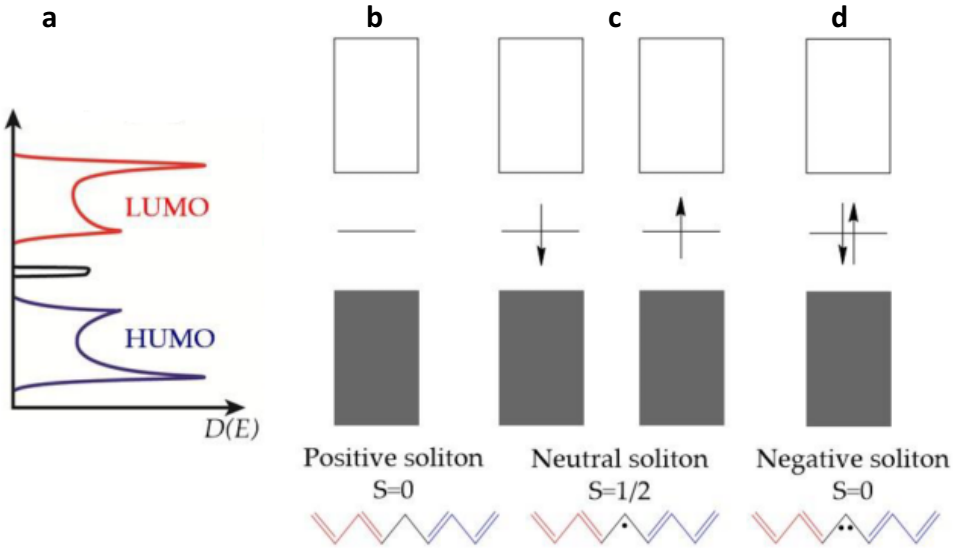


Figure 1-4: a) The midgap introduced by excess of charges into trans-polyacetylene; b) an empty positive soliton; c) a neutral soliton that can be characterised either by an electron having a downward or upward spin; d) a doubly negative soliton. Taken from[48].

Solitons electronic energy lies in the middle of the π-π* gap so introducing a possible midgap optical transition in addition to the π-π* one [43], [48] (Figure 1-4 a). On trans-polyacetylene, soliton can result as: a doubly occupied negatively charged soliton S- (Figure 1-4 d); an empty positively charged soliton S+ (Figure 1-4 b); a neutral soliton S as a consequence of one electron occupying the soliton state (Figure 1-4 c) [49]. Conjugated polymers not featuring a doubly degenerate electronic ground state, i.e. characterised by a lower energy benzenoid state and a higher energy quinoid state as in polyphenylene vinylene, result altered in their bond-alternation pattern by excess electronic charge. Since the alteration induced is forcing the system to acquire an energetically disfavoured status, the distortion is strongly localised on the chain. Such alteration is called *polaron* and can be seen as a charged quasi-particle that strongly interacts with the surrounding lattice. Polarons are equivalent to a pair of localised solitons interacting and forming bonding/anti-bonding combinations of solitons. In the presence of a doubly degenerate electronic state polarons decay into a soliton. Polarons can accommodate up to 4 electrons, so generating four different polaron kinds: negative polarons p-; negative bipolarons bp^{2-} ; positive polarons p+; positive bipolarons bp^{2+} (Figure 1-5).

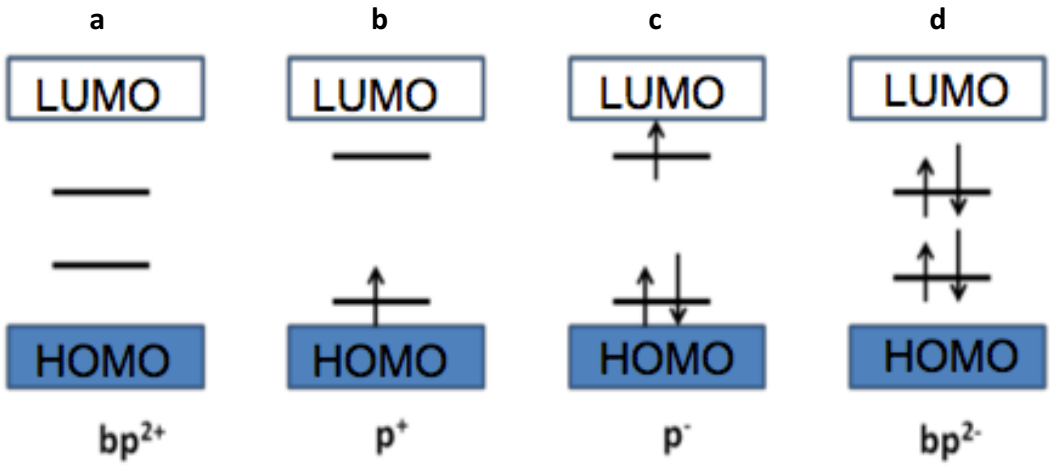


Figure 1-5: Formation of positive bipolarons (a), positive polarons (b), negative polarons (c) and negative bipolarons (d) upon occupation of polaron states by electrons.

Upon photoexcitation of CPs so-called *excitons* are formed, namely neutral quasi-particles of electron-hole pairs characterised by a binding energy (BE) due to the Coulombic attraction between them and by diffusion lengths dependant on the charge screening of the material in which excitons are formed, that in turn depend on the dielectric constant of the same. Materials featuring a relatively low dielectric constant (ε = 2-4), as in CPs, form excitons classified as *Frenkel excitons* characterised by a BE ranging between 0.2 eV and 1.5 eV and a diffusion length of the order of 10 nm[50]. On the contrary, in materials featuring a relatively high dielectric constant the charge screening is stronger, as inorganic semiconductors, and generated excitons are so-called *Wannier-Mott excitons* that are characterised by a BE of the order of few meV and diffusion lengths of tens of the lattice constant (i.e. >100 µm in single crystalline systems for inorganic semiconductors). The localisation of charge causes transport to occur via hopping, i.e. thermally-assisted tunnelling between localised sites. Such transport is favoured by phonons scattering so determining mobility of CPs to be strongly affected by temperature and to increase with the latter raising, contrarily to inorganic semiconductors, according to the exponential law:

$$\boldsymbol{\mu = \mu_0 e^{-\left(\frac{T}{T_0}\right)\alpha}} \qquad \textbf{(Equation 1-1)}$$

where μ_0 is the pre-exponential factor representing the hopping mobility in absence of energetic disorders, T_0 is an empirical parameter related to the Gaussian width of the site distribution, α is an integer of a value between 1 and 4 and T is the temperature. At room temperature µ is between 0.1 cm^2/Vs and 2.5 cm^2/Vs for disordered CPs, whilst it is considerably higher in molecular crystals (up to 20 cm^2/Vs) [43], [51], [52].

1.1.2 Optical properties of CPs

Upon photo or electric stimulation excitons arise in CPs. In the case of photoexcited excitons, an electron is promoted to an excited state, whereas in the case of electrically excited excitons a mutual capture of free charges within close proximity takes place. Depending on the spin angular momentum S as a combination of the spin of the electron and the hole involved, these excitons can be *singlets* (S=0) or *triplets* (S=1) [50], [53]. Excitons formed via photoexcitation are primarily singlets and they can decay by means of a radiative or non-radiative process. Instead, electrically stimulated excitons can form either singlets or triplets according a 1:3 ratio and undergo radiative or non-radiative decay [49], [54] (Figure 1-6). In radiative decay, the excited electron of a exciton releases the acquired energy surplus by emitting a photon while retroceding toward a lower energy state [44].

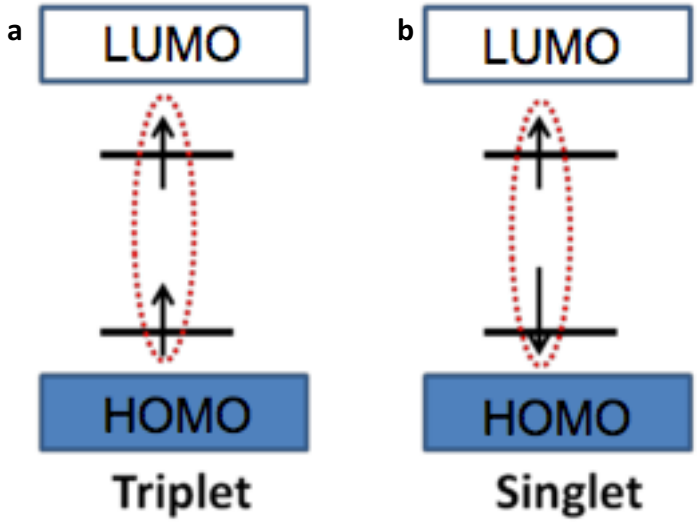


Figure 1-6: (a) A triplet, characterised by the electron and the hole having parallel spins, (b) a singlet characterised by the electron and the hole having antiparallel spins.

The processes involved in light-absorption and in light-emission are generally described by so-called *Jablonski diagram* (Figure 1-7). The electronic energy levels are vertically arranged and named S_0 (ground state), S_1 (first excited state), S_2 (second excited state) and T_1 (triplet state). Electronic energy states are organised in subsystems called vibrational levels approximately spaced 0.1 eV from each other, a gap much lower than the one between electronic (excited and ground) states. Radiative processes are indicated by means of green arrows whilst non-radiative ones by means of dashed lines.

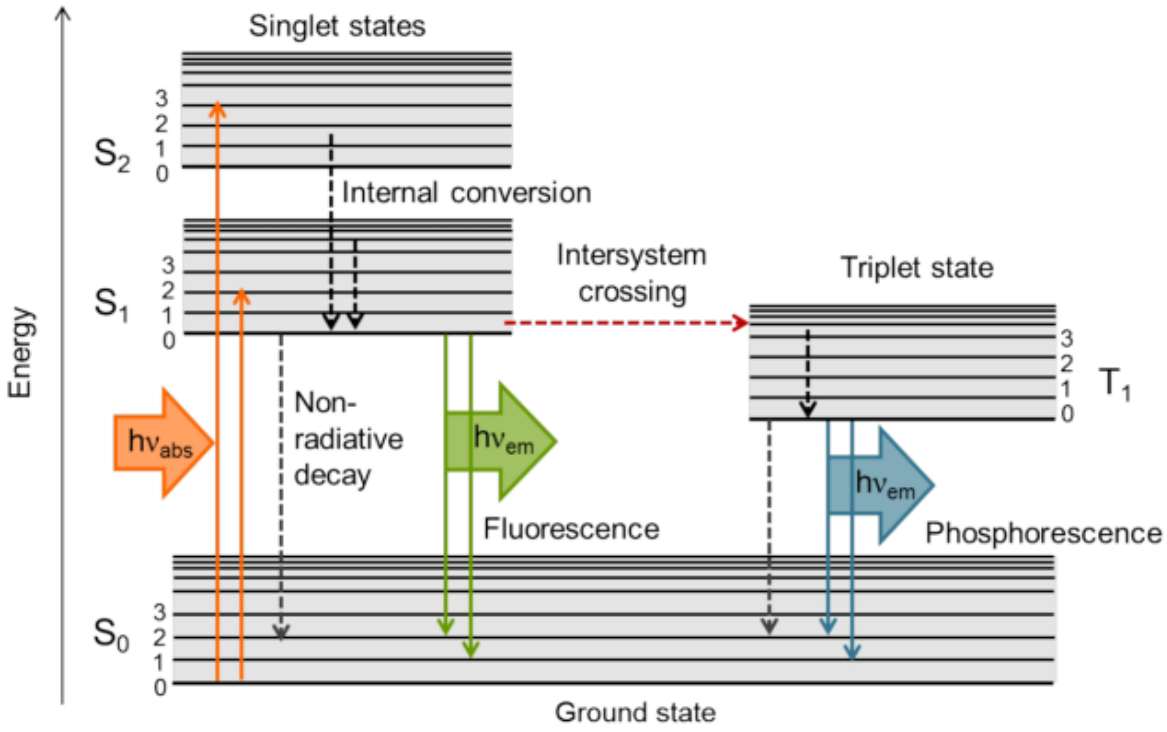


Figure 1-7: Jablonski diagram: S0, S1 and S2 are the ground state, the first and second excited state respectively. T1 indicates a triplet state. Radiative decays are represented with solid lines whilst non-radiative decays with dashed lines. Taken from[55].

Absorption, ($h\nu_{abs}$ in Figure 1-7) is a vertical transition from S_0 to S_1 or S_0 to S_2 and occurs within 10^{-15} s. Both S_1 and S_2 are excited singlet states. Electrons moved from S_0 to S_2 relax firstly to S_1 by internal conversion within 10^{-12} s. Electrons in S_1 relax to S_0 via internal conversion so that a relaxation from the lowest vibrational level of S_1 is most likely to take place rather than from other vibrational states of the same excited state. Once in S_0, electrons, in vibrational levels higher than the lowest one, relax further to eventually end up in the lowest vibrational level within 10^{-12} s. The radiative decay taking place upon the relaxation from an excited state to the ground state is called *fluorescence* and occurs within an elapse of nanoseconds ($h\nu_{em}$ in Figure 1-7). State T_1 is involved in intersystem crossing, namely a process involving an intermediate state necessary for triplets to rearrange parallel spins (total spin momentum = 1) into antiparallel ones (total spin momentum = 0) so that exciton can return to the ground state, where only excitons with a null total spin momentum are allowed. Such process occurs within microseconds to milliseconds, a considerably longer period of that observed for singlets emission (that is of the order of nanoseconds), and is referred as *phosphorescence*. Upon photoexcitation, the combination of the occurring phenomena of fluorescence and phosphorescence is termed *photoluminescence* (PL) [56]–[58].

1.2 Optoelectronic devices

CPs have found an extensive utilisation in optoelectronic devices, as previously said, because of the multiple properties they feature (lightweight, cheap production costs, easy manufacturing, biocompatibility, flexible and stretchable mechanical properties[5], [12], [59]–[61]) and the potential scenarios they open in application fields such as medicine [62]–[64], robotics [13] and space technology [10]. The CPs-based devices that have been studied the most are OPVs, OLEDs and OFETs. In this section, the main aspects of these three devices typologies are described.

1.2.1 Organic photovoltaics (OPVs)

CPs are extensively used in photovoltaic solar cells as active layer. The latter can be obtained either as a blend (in case of bulk heterojunction solar cells) or as a bilayer (in case of a planar solar cells) of an *electron donor* polymer, such as polythiophene (e.g. P3HT or PBTTT), and an *electron acceptor* polymer, such as fullerene derivative (e.g. PCBM) [65], [66]. Upon photo-stimulation, excitons are formed in the active layer of these devices. OPVs are aimed to convert photons on electric current, the generation of which stems from the splitting of exciton holes from the corresponding exciton electrons so as to obtain charges to flow through the device layers and, eventually, to be collected at the electrodes. The photovoltaic hole-electron splitting process[67] is described in Figure 1-8 and consists in:

i. Generation of excitons (electron/hole pairs bounded by Coulomb force) upon photon absorption by electron donor polymers;

ii. Dissociation of excitons into free charges at the donor/acceptor interface;

iii. Charge transport across the active layer;

iv. Charge collection at the electrodes.

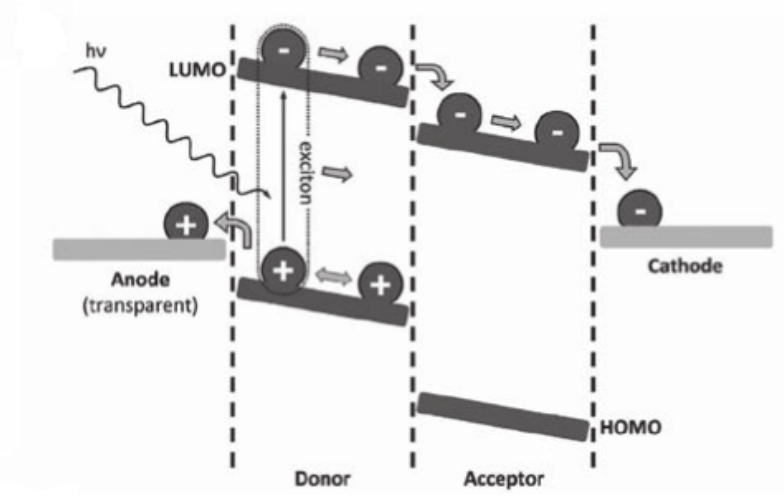


Figure 1-8. Simplified mechanism of OPV exciton dissociation. Taken from[67]**.**

OPVs are characterised by a multi-layered structure. Depending on the position of the electrode from which electrons are extracted, it is possible to obtain a *direct structure* (electrons extracted from metallic electrode) or an *inverted structure* (electrons extracted from the conductive thin-oxide electrode). The positions of each layer in both configurations can be summarised as in Figure 1-9): i) top metal electrode; ii) electron-collection layer (ECL) (direct structure) or hole-collection layer (HCL) (inverse structure); iii) the active layer in which excitons formation occurs upon photo-excitation; iv) HCL (direct structure) or ECL (inverse structure); v) transparent conductive oxide (TCO) as bottom electrode coated over a transparent substrate (silica or glass) from which light reaches the active layer. The active layer can be obtained by either arranging an electron-donor and an electron-acceptor according a *planar heterojunction* (or type I), i.e. by depositing a film of one of the two materials first and the other on top afterwards, or according a *bulk heterojunction* (BHJ) (or type II), namely by obtaining a blend of the two materials to be deposited as unique film. The bulk heterojunction has been demonstrated to maximise the contact surface between the two components of the active layer, therefore obtaining a higher number of dissociated charges at the donor/acceptor interface than the planar heterojunction [66], [68], [69].

In this thesis, the treated OPVs were all built according the direct structure and by using this material sequence: ITO/PEDOT:PSS/P3HT:PCBM/Ca/Al. ITO (Indium Tin Oxide) acts as bottom TCO (anode), poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) is the HCL, the blend P3HT:PCBM is the active layer and the Ca/Al is the top metallic electrode (cathode). The active layers

of OPVs are mostly obtained out of a solid blend composed by an electron-donor and an electron-acceptor material. Such configuration is therefore a bulk heterojunction (BHJ) and features a nanostructured morphology formed by spontaneous phase separation between the two components[70], [71]. The typical exciton diffusion length in CPs is ~ 10 nm, as seen before, hence the length scale of such phase separation should be within 10-20 nm. Furthermore, a highly interpenetration between the two blend components maximise the overall interface area in correspondence of which the charge splitting takes place. An opportune choice of materials with properly matching donor and acceptor LUMO-HOMO levels (Figure 1-10) renders OPVs capable to generate current upon photo-stimulation. In P3HT:PCBM OPVs, P3HT acts as electron donor whilst PCBM as electron acceptor[66].

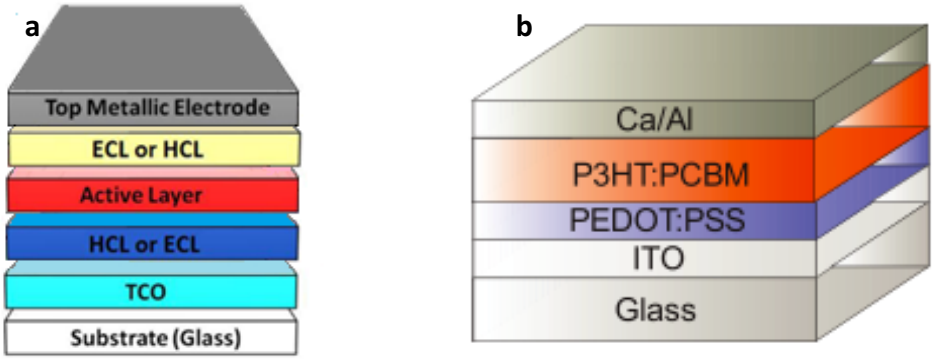


Figure 1-9: (a) The general structure of an OPV. (b) The direct structure normally used to build P3HT:PCBM BHJ OPVs. Taken from[72].

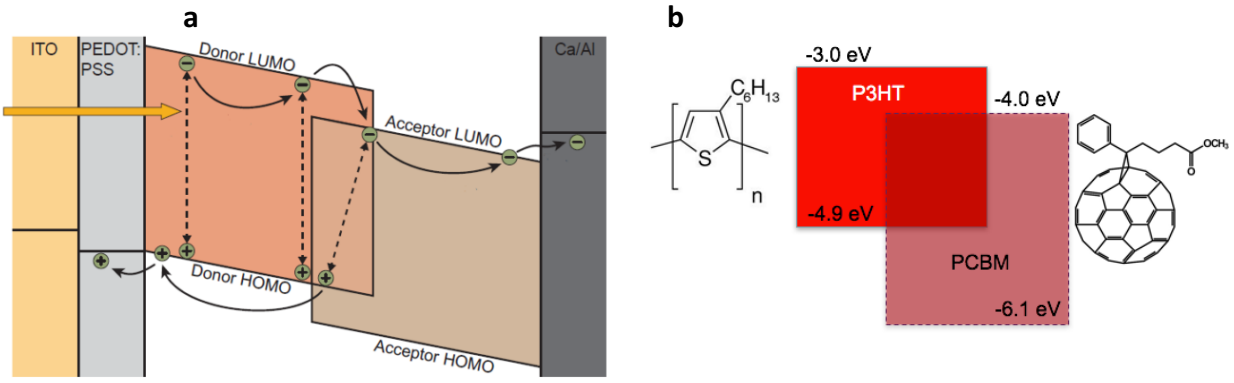


Figure 1-10: (a) The occurring charge splitting and electrodes collection taking place in a BHJ P3HT:PCBM OPV. In order to be split into free charges, the exciton has to diffuse at the electron-donor/electron acceptor interface within its lifetime. Once split, charges travel through electrodes favoured by the built-in field due to the energy band configuration. Taken from[47]. **(b) P3HT:PCBM as an example of a proper donor/acceptor HOMO-LUMO level matching to obtain charge splitting upon photo-excitation.**

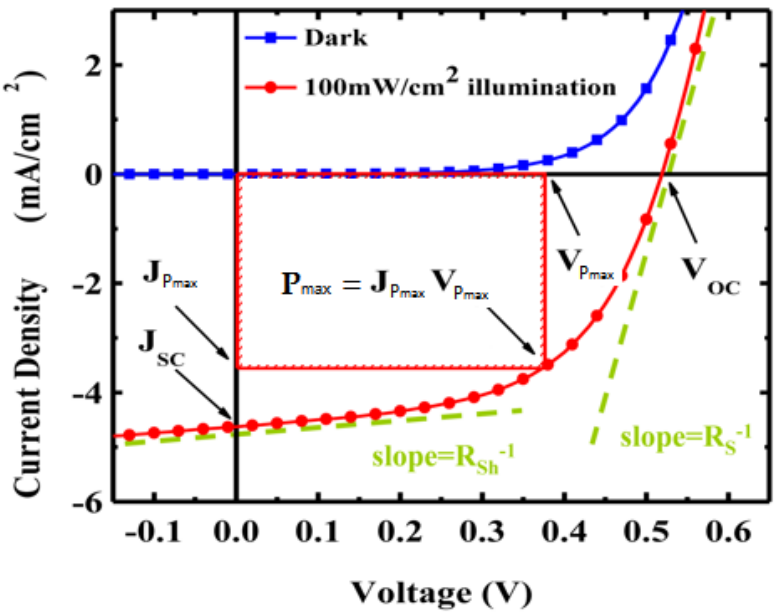


Figure 1-11: The JV curves of a solar cell under illumination conditions equivalent to 1 Sun (100 mW/cm²) (red line) and in dark conditions (blue line). The J_{SC}, the V_{oc}, the J_{pmax}, the V_{pmax} and the P_{max} points are highlighted. R_{sh} and R_s are respectively the shunt-resistance and the series resistance of the equivalent circuit of the solar cell. Adapted from[73].

The current density vs voltage (JV) curve characterisation of OPVs under both illumination and dark conditions give meaningful insights about a cell functionality. A typical JV curve is reported in Figure 1-11 from which it is possible to extract the parameters normally used to assess a cell quality, namely the *short-circuit current density* (J_{sc}) and the *open-circuit voltage* (V_{oc}). The J_{sc} is the current measured under illumination conditions with no external applied voltage, i.e. in correspondence of the conditions the diode delivers the maximum current. This parameter mainly depends on three factors: i) the fraction of absorbed photons, in turn depending on the absorption spectrum, on the absorption coefficient and on the thickness of the absorbing layer; ii) the fraction of dissociated excitons that is depending on the phase separation between the two blend components, required to match the exciton diffusion length; iii) the fraction of charges successfully reaching the collecting layers with respect to those lost for recombination due to charge traps or impurities present throughout the active layer.

The open circuit voltage (V_{oc}) is the value of applied voltage capable of null the built-in voltage due to the different HOMO level of the donor and the LUMO level of the acceptor. In correspondence of such value the current flowing through the device is zero. The V_{oc} can be therefore directly obtained according the following formula:

$$V_{oc} = \frac{1}{e}\left(\left|E_{HOMO}^{donor}\right| - \left|E_{LUMO}^{acceptor}\right| - 0.3\ eV\right) \qquad \text{Equation 1-2}$$

where e is the elementary charge and E is the energy level. The empirical factor 0.3 eV is a correction of a deviation arising because of factors such as charge mobility and active layer thickness [74]. For a P3HT:PCBM OPV the calculated V_{oc} is 0.6 eV, however, the measured one is 0.56 eV. Such discrepancy stands because of the dependency of V_{oc} not only on the HOMO and LUMO values but also on the quality of the electrode/active layer interfaces, as the presence of defects at the interfaces or short circuit pathways (i.e. pinholes or cracks in the active film) lead to an increase of the resistivity offered by the material, and thus, to a lowering of the V_{oc} [75]–[77]. Importantly, the V_{oc} turns to be a valuable factor to assess the cell overall conditions since a close value of the measured-V_{oc} to the calculated-V_{oc} points out a good charge transport along cell layers. The JV curve also indicates the point corresponding to the maximum power provided by the solar cell, i.e. the P_{max}, obtained as the product of the current density J_{pmax} and the voltage V_{pmax} (Figure 1-11). A fundamental parameter calculated starting from the J_{sc}, the V_{oc} and the P_{max} is the so-called *fill-factor* (FF), used to directly measure the squareness of the JV curve:

$$FF = \frac{P_{max}}{V_{oc} * J_{sc}} = \frac{V_{pmax} * J_{pmax}}{V_{oc} * J_{sc}} \qquad \text{Equation 1-3}$$

FF value is between 0 and 1, an ideal cell would have a FF of 1, hence giving its maximum power in correspondence of the J_{sc}. However, such condition cannot be satisfied and real cells feature a FF lower than 1. The yield of the solar cell in terms of incident power P_{in}, due to the light converted in delivered current, is measured by the *power conversion efficiency* (η) obtained as:

$$\eta = \frac{P_{max}}{P_{in}} = FF * \frac{V_{oc} * J_{max}}{P_{in}} \qquad \text{Equation 1-4}$$

The power conversion efficiency is measured by adopting as standard conditions a temperature of 25 °C and a light source characterised by an intensity of 1 sun, equivalent to 1000 W/m^2, and a solar spectral distribution of 1.5 AM (air mass), equivalent to the irradiance and spectrum of incidental solar ray in a 48.2° angle[78].

The equivalent circuit model for a solar cell[79], [80] (Figure 1-12) consists of a current generator I_L that takes in account the photo-generated current flowing through the device, of a current I_D produced by a diode that takes in account the recombination of the charges and the dark current that would flow in the opposite direction of the I_L, a shunt-resistance R_{SH} parallel to the diode that considers the resistance across the active layer and a series resistance R_s that takes in account the loss due to the contacts. As shown in Figure 1-11, R_{sh} affects the slope of the straight line tangential

to the JV curve in the 0 V - V_{Pmax} portion, whereas R_s affects the slope of the straight line tangential to the JV curve from V_{oc} onwards[73].

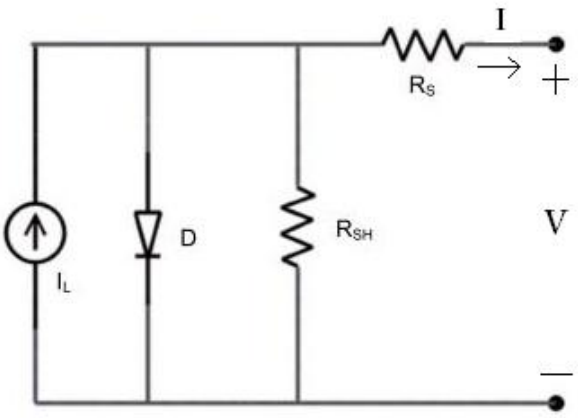


Figure 1-12: The equivalent circuit of a solar cell.

The equation describing the output current I is:

$$I = \frac{R_{SH}}{R_{SH}+R_S}\left[\left(I_L - \frac{V}{R_{SH}}\right) - I_{D0}\left(\exp\left(\frac{V+IR_S}{nKT/q}\right) - 1\right)\right] \qquad \textbf{Equation 1-5}$$

That, in correspondence of the V_{oc}, becomes

$$V_{oc} = \frac{nKT}{q} ln\left(\frac{I_L - V_{oc}/R_{SH}}{I_{DO}} + 1\right) \qquad \textbf{Equation 1-6}$$

whereas, in correspondence of the short circuit current (I_{sc}), 1-5 becomes:

$$I_{SC} = \frac{R_{SH}}{R_{SH}+R_s}\left[I_L - I_{D0}\left(exp\left(\frac{I_{Sc}R_S}{nKT/q}\right) - 1\right)\right] \qquad \textbf{Equation 1-7}$$

The current I, the short circuit current I_{sc} and the I_{pmax} can be expressed as J, J_{sc} and J_{pmax} simply dividing the current values by the solar cell pixel area.

1.2.2 Organic light-emitting devices (OLEDs)

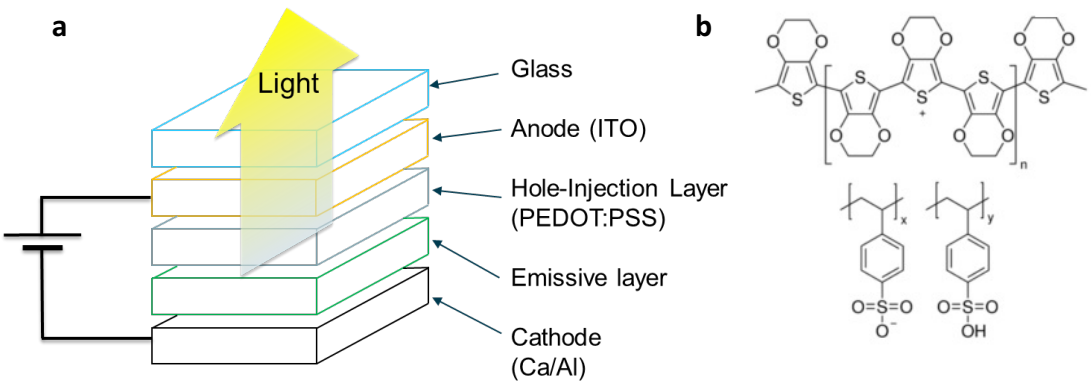


Figure 1-13: the structure of a OLED (a) and the hole-injection layer (HIL) PEDOT:PSS (b).

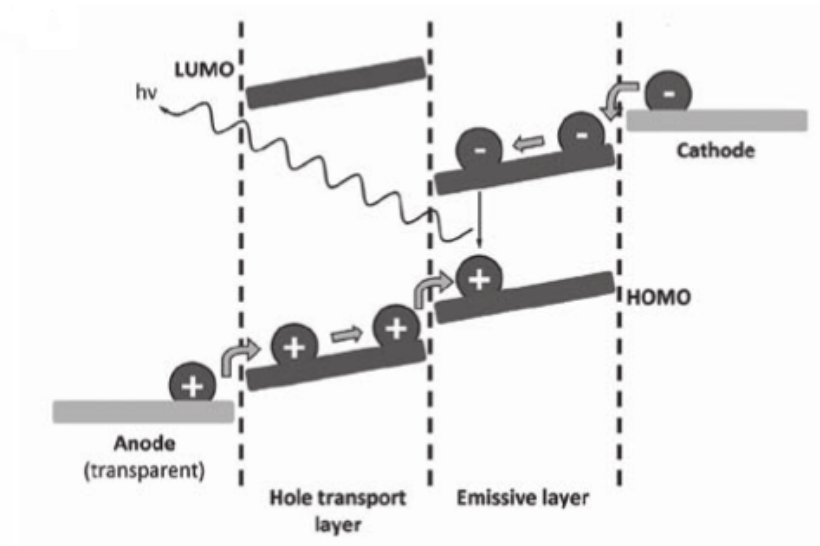


Figure 1-14: Injection and recombination of charges in OLEDs and subsequent photon emission. Taken from[67].

In OLEDs the recombination of electrons and holes, induced upon an electrical stimulation, is aimed at the emission of photons, the emission frequency of which depends on the energy gap of the active layer. The main phenomena occurring in OLEDs upon electrical stimulation are[67] (Figure 1-14):

i. Injection of charge carriers, namely electrons in the LUMO of the organic layer from the cathode and of holes at the HOMO of the organic layer from the anode;

ii. Carrier transport through the device and formation of excitons into the active layer;

iii. Electrostatic interaction and consequent combination of electron-hole pairs to form excitons, or bound hole-electron pairs;

iv. Radiative emission upon recombination, by means of photons.

A well-established structure for an OLED consists of a thin film of an organic semiconductor, i.e. the *emissive layer* (∼100 nm), sandwiched between two electrodes. A hole-injection layer (HIL) can also be inserted between the anode and the emissive layer as well as electron-transport layer (ETL) to improve charge injection into the device (Figure 1-13a). The structure is very similar to the one already observed for OPVs (1.2.1) with a TCO (anode) on one side to allow light to be emitted and a metal on the other side (cathode). The TCO must feature high transparency, low sheet resistance, low roughness and a high work function. For both OPVs and OLEDs the TCO chosen to build the devices discussed in this thesis is indium-tin-oxide (ITO) (In_2O_3 (90 wt%) and SnO_2 (10 wt%) that has a good transparency (up to 90% at 550 nm), a low sheet resistance (∼20 Ω/□), a low roughness (∼3 nm rms) and a high work function (∼4.6 eV). Furthermore, PEDOT:PSS (poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate)) (Figure 1-13b) is used as HCL in OLEDs. Notably, the same material is also used as HIL in the OPVs in this thesis studied, since in both cases PEDOT:PSS enhance the charge transport between the active layer and the anode (i.e. the TCO).

In OLEDs, PEDOT:PSS provides a low barrier for hole-injection given that the HOMO of the emissive layer is normally between 5 eV and 6 eV. Furthermore, ITO featuring a work function of ∼4.6 eV, which is generally increased to ∼4.7-4.8 eV by means of an oxygen plasma treatment, further lowers the barrier to the injection of holes from the anode. Analogously, in OPVs, PEDOT:PSS provides a low barrier for hole-extraction from the donor HOMO to the ITO anode. Other two analogies between OPV and OLED structures are: i) the oxygen plasma treatment these devices undergo to increase the work function (∼4.7-4.8 eV), lower the sheet resistance (∼15 Ω/□) and decrease surface roughness (from 3 nm to 1.4 nm rms) of ITO [38], [81]; ii) the choice to use a low work function material for the cathode in order to reduce electron injection/collection (OLEDs/OPVs) barrier since LUMO of the emissive/acceptor (OLEDs/OPVs) layer is typically 2-3 eV. Concerning ii, for both OLEDs and OPVs here studied a thin layer of calcium (∼30 nm) capped with

aluminium (∼150 nm) is used as cathode. Ca has a work function of ∼2.8 eV whereas Al of 3.7-4.2 eV. The active layer chosen for the OLEDs in this thesis studied is F8BT (poly(dioctyfluorene-alt-benzothiadiazole))[82], [83].

OLEDs exploit so-called *electroluminescence* (EL) phenomenon, namely the emission of a photon upon recombination of an injected electron (from the cathode) with an injected hole (from the anode) taking place in the emissive layer. In fact, injected charges establish excitons as result of the coulombic interaction between an injected-electron in the LUMO of the active material and an injected-hole in the HOMO of the same. Excitons may decay radiatively or non-radiatively afterwards.

The light emitted and measured from OLEDs can be expressed either in *radiometric* or *photometric* units. Radiometric units count the number of photons emitted by the device, whereas photometric units express the light emission according to the sensitivity of the human eye giving the actual brightness perceived by the eye. However, the latter is restricted to the visible part of electromagnetic spectrum, i.e. 400 nm to 700 nm. Whenever the light emission falls outside such range, it must be expressed in radiometric units and the emission intensity is given as radiance (W sr^{-1} m^{-2}).

OLEDs are normally assumed as Lambertian light sources, or rather a source having the same radiance in any direction. The corresponding photometric unit for the radiance is the luminance ($cd \cdot m^{-2}$). F8BT emits in the visible range, therefore OLEDs studied in this thesis are characterised according photometric units, i.e. current density-luminance vs voltage (JLV) and EL vs voltage graphs (Figure 1-15). Upon application of a voltage bias between the anode and the cathode, the parameters normally used to characterise OLEDs functionality are: i) *the turn-on voltage* (V_{ON}), namely the (arbitrarily defined) bias required to obtain an emitted intensity equal to ∼5 times the value of the intercept of the LV curve (cd/m^2) with the noise level in the semi-log plot [44], [84] (Figure 1-15b); ii) *the external quantum efficiency* (EQE), namely the ratio between the photons emitted and the charges injected; iii) the *EL maximum wavelength of emission* (λ_{max}) (Figure 1-15a).

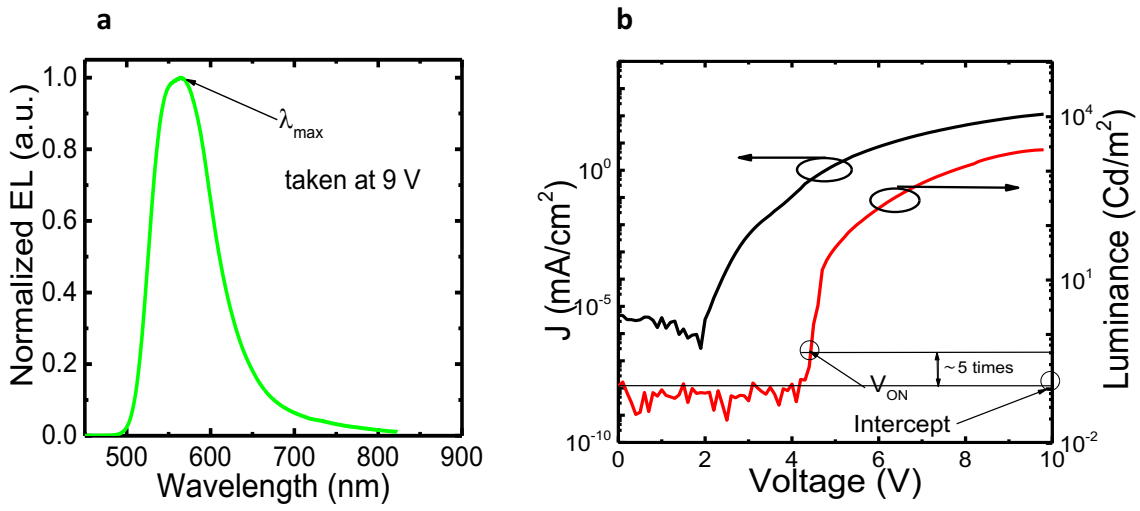


Figure 1-15: The EL vs voltage (a) and the JLV graph (b) of a F8BT OLED built for the purposes of this thesis. The EL spectra were collected by applying a 9 V bias between the anode and the cathode.

The V_{ON} value is affected by the presence of charge traps, impurities and device degradation due to oxidation. The EQE is the most important parameter to assess the efficiency of a LED and can be calculated as:

$$EQE = \eta_{PL} * r_{st} * \gamma * \eta_{out} \qquad \text{Equation 1-8}$$

where: η_{PL} is the photoluminescence quantum efficiency; r_{st} is the ratio between singlets and triplets, normally 0.25 [49], [54]; γ is the charge balance factor and takes in account the number of excitons generated per electrons injected in the device; η_{out} is the light out-coupling efficiency [38], [85] that measures the amount of internally generated light escaping from the device and limited by the difference in the refractive indices between layers and other factors such as the total internal reflection at the glass/air interface. Out-coupling efficiency can be as low as 19 %, meaning that up to almost 80 % of the light can be lost in waveguiding in the device[86].

1.2.3 Organic Field-Effect Transistors (OFETs)

OFETs, similarly to other CPs-based devices, can be integrated in plastic low-cost circuits[9], [87], [88]. A plethora of CPs have been investigated and applied as active layer for such device, such as poly(alkylthiophenes), liquid-crystalline thieno-thiophene copolymers and indacenodithiophene–benzothiadiazole copolymers, exhibiting mobilities ranging from 0.1 $cm^2V^{-1}s^{-1}$ to 5 $cm^2V^{-1}s^{-1}$[89]–[91].

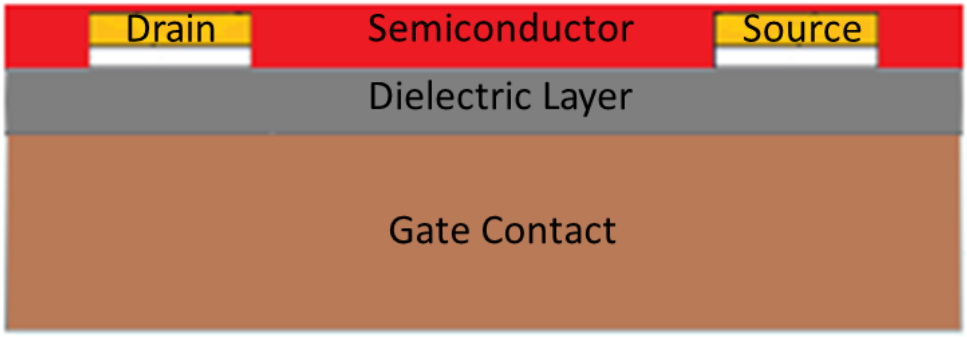


Figure 1-16: The generic structure of a OFET: two upper metallic contacts act as drain and source contacts; an extended gate contact, usually obtained by heavy n-doping of Si, located on the bottom of the device; a dielectric layer located in the middle of the structure and electrically isolating the gate contact from the upper contacts; a semiconductor layer deposited at the top of the whole structure and immerging the drain and the source contacts.

A typical OFET structure (Figure 1-16) is characterised by: i) a semiconducting layer; ii) a dielectric layer; iii) two electrodes called source (S) and drain (D) usually located on top of the dielectric layer aimed at enabling charge injection and extraction; iv) a gate (G) electrode located on the bottom of the dielectric layer aimed at modulating the resistance of the semiconductor layer immediately laying at the interface with the dielectric material, properly termed transistor channel. The semiconductor is the active layer of the device and provides, upon the proper applied bias between the gate and the source contacts (V_{GS}), a conductive channel enabling charge injection from the drain and charge extraction from the source. Drain and source contacts create ohmic contacts with the semiconductor, and thus, with the arisen channel. A crucial difference with inorganic field-effect transistor such as metal-semiconductor FETs (MESFETs) or metal-insulator FETs (MISFETs) consists in the absence of an inversion regime for OFETs while they can operate in accumulation or depletion regime[92]. The accumulation arises upon an applied negative bias on the gate contact so turning the dielectric capacitive layer negatively charged and therefore attracting the majority holes (p-OFETs) to the semiconductor-insulator interface that create a so-called *channel*. A DS positive current (holes) therefore flows through this channel and it is modulated by the gate voltage. A depletion regime arises upon the application of a small positive bias to the gate electrode so causing the repelling of majority carriers from the semiconductor-insulator interface [93]. In this thesis, the analysed semiconductors are either P3HT or PBTTT (Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene)) OFETs, both p-type transistors. OFETs reported in the literature are mostly based on CPs featuring a p-type behaviour [92], [94], since the n-type behaviour is affected

by e-trapping at the semiconductor-dielectric interface by hydroxyl groups (silanols in the case of SiO_2 dielectric as those growth in the substrate used to build the OFETs in this thesis analysed). Nevertheless, n-type OFETs are obtained by using CPs featuring high electron mobility such as 8_3-NTCDI (N,N -bis (3-(perfluoroctyl)propyl)-1,4,5,8-naphthalenetetracar-boxylic acid diimide) and by means of superficial treatments aimed at reducing the e-trapping, such as self-assembled monolayers (SAMs) coating the dielectric layer[91],[92]. In n-type OFETs the required bias to open the channel must be positive so as to positively charge the dielectric capacitance and therefore obtain an accumulation of electrons at the semiconductor-insulator interface. Importantly, n-type transistors can also be achieved by using P3HT or PBTTT but, since the electron mobility in these devices is approximately tenfold lower than the hole one (hole/electron mobility in P3HT ~0.01 $cm^2V^{-1}s^{-1}$/~0.001 $cm^2V^{-1}s^{-1}$; hole/electron mobility in PBTTT ~1 $cm^2V^{-1}s^{-1}$ / ~0.1 $cm^2V^{-1}s^{-1}$), p-type OFET behaviour better suits these CPs [97].

The characterisation of OFETs requires measuring the current vs voltage curves (IV) that can be either the drain-source current (I_{DS}) vs the gate-source voltage (V_{GS}) curve, termed *transfer characteristic*, or the I_{DS} vs the drain-source (V_{DS}) curve, termed *output characteristic*. The transfer characteristics are taken by using the applied V_{DS} as parameter, whereas the output characteristics are measured by using the applied V_{GS} as parameter. Hence, IV curves of OFETs are normally reported as a collection of several transfer characteristics and of output characteristics (Figure 1-17). When no bias is applied the transistor is in the so-called *off state*, whereas it is in the *on state* for an applied bias capable to open the device channel.

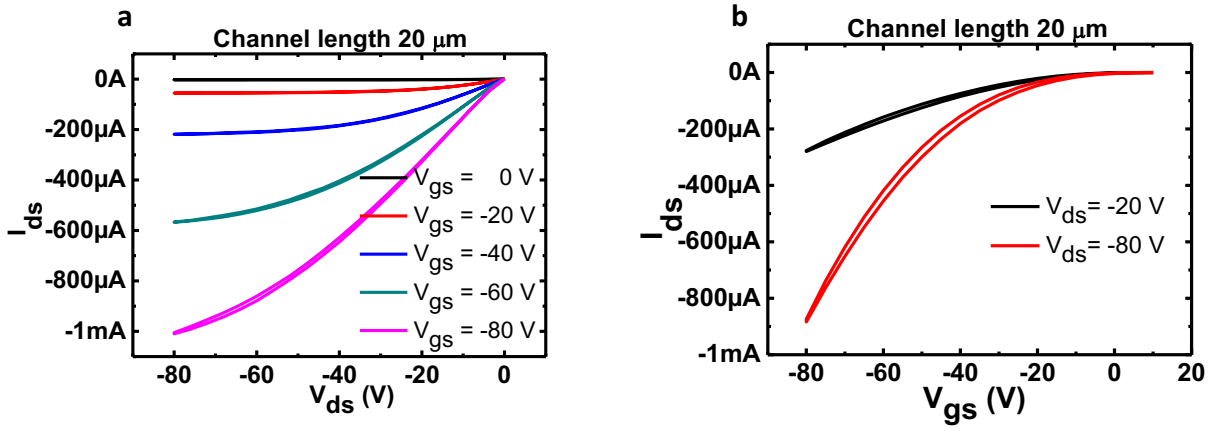


Figure 1-17: The output characteristics (a) and the transfer characteristics (b) of a PBTTT OFET featuring a channel length of 20 μm. The V_{GS} used as parameter in the output curves was ranging between 0 V and -80 V according an increasing step of -20 V. The V_{DS} in the transfer characteristics was ranging between -20 V and -80 V with an increasing step of -60 V.

For an applied V_{GS} higher than the applied V_{DS}, OFETs work in so-called *linear regime* ($V_{GS}>V_{DS}$) where I_{DS} can be expressed as:

$$\boldsymbol{I_{DS} = \frac{W}{L} * \mu * C_i * \left[\left(V_{GS} - V_{TH} \right) * V_d - \frac{{V_{DS}}^2}{2} \right]} \qquad \textbf{Equation 1-9}$$

where W and L are respectively the width and the length of the transistor channel, μ is the mobility of charge carriers within the channel, C_i is the capacitance per unit area of the insulating layer of the transistor, V_{TH} is the so-called *threshold voltage*, or rather the minimum bias voltage necessary to induce a conductive channel [98]. For an applied V_{GS} lower than the applied V_{DS}, OFETs work in so-called *saturation regime* ($V_{DS}>V_{GS}$), in correspondence of which a depletion layer extends for the whole semiconductor thickness[98], and the equation 1.9 becomes:

$$\boldsymbol{I_{DS} = \frac{W}{2L} * \mu * C_i * \left(V_{GS} - V_{TH} \right)^2} \qquad \textbf{Equation 1-10}$$

The last equation is normally used to assess both the V_{TH} and the mobility μ. In fact, the threshold voltage V_{TH} can be extracted by determining the x axis intercept of $(I_{DSsat})^{1/2}$ vs V_{GS} in the saturation regime(equation 1.10)[99], whilst μ corresponds to the slope of such graph (Figure 1-18). The threshold voltage can also be expressed as:

$$\boldsymbol{V_{TH} = \pm \frac{q n_0 d}{C_i} + V_{fb}} \qquad \textbf{Equation 1-11}$$

where V_{fb} is the flat-band potential that takes in account any work-function difference between the semiconductor and the gate metal, q is the elementary charge, n_0 is the density of free carriers whereas d is the semiconductor thickness. The sign of the right-hand side of the equation depends on the sign of the charge carriers.

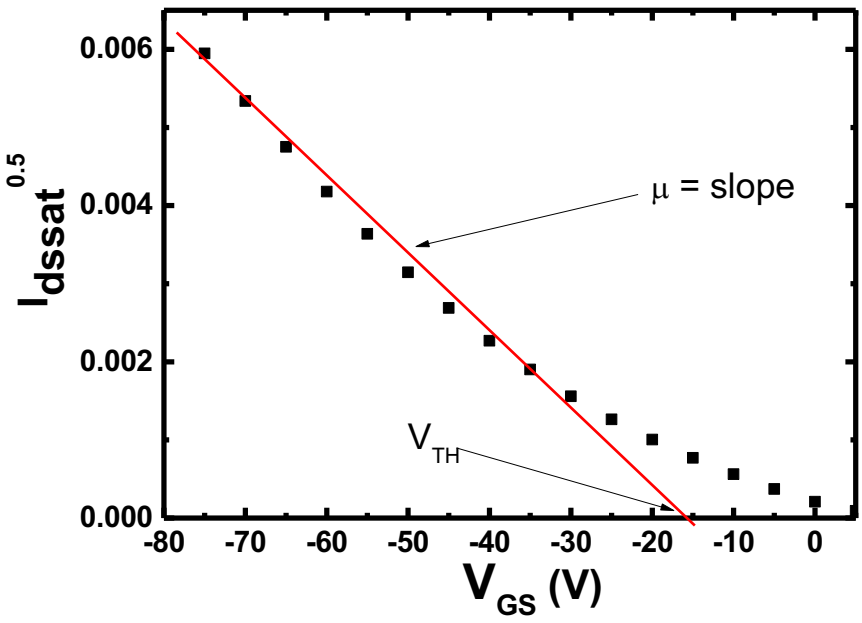


Figure 1-18: The $I_{DS}^{0.5}$ vs V_{GS} graph of a OFET built for the purposes of this thesis used to extract both V_{TH} and μ.

The electrical parameters useful to assess OFETs performances are: i) *the field-effect charge carrier mobility* μ; ii) the V_{TH}; iii) the *on/off current ratio*, i.e. the ratio between the I_{DS} value for V_{GS}=0 and V_{GS}=V_{DS} measured over the same transfer characteristics, hence for the same applied V_{DS}. In fact, mobility and V_{TH} can be affected: by the presence of traps at the insulator-semiconductor interface resulting in a variation of n_0; by C_i alterations due to charge injection from the gate or the drain/source; by structural variations affecting the V_{fb}[93], [99]. Importantly, mobility depends on the magnitude of the gate voltage and therefore is field-effect dependent. The on/off ratio is a figure of merit for OFETs since higher values of this parameter results in a better switch between a condition of off state, hence with the solely sub-threshold voltage flowing between drain and source, to an on state in which considerable higher current flows within the device. Such parameter, in fact, establishes the quality of the OFET to act as a switch, particularly important for applications in digital circuits, and to determine a low consumption in correspondence of circuit standby. A variation of the V_{TH} or an increase of the charges trapped within the device can alter such parameter.

1.3 Electrostatic Discharge (ESD)

Damages prevention due to *electrostatic discharge* (ESD) in electronic circuits relies on the utilisation of circuit (or component) protections. The latter are designed according to specifications that can be obtained by means of a *transmission line-pulsing* (TLP) system, which is aimed to reproduce on workbench ESD phenomena[14], [100]. Such technique is widely used to test inorganic electronic circuits aimed to be used on a large scale, such as phones, TVs, laptops etc. [16], [101]–[103]. Interestingly, TLP testing has been poorly applied on organic devices since only few papers have been reported so far on the subject, and thus, the characterisation of the TLP-stress response of organic devices turns out particularly important for a large-scale deployment.

1.3.1 Transmission-Line Pulse

ESD events normally occur in daily life due to the tendency of bodies to get charged, because of friction, and to discharge over other not-charged or grounded objects. There are several possible ESD mathematical models such as Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM), Charge Board Model (CBM), Human Metal Model (HMM), Cable Discharge Events (CDE) and others[104]–[106]. In these, human body, machines, IC chips, circuit boards, cables, or an entire system are modelled by a RC or RLC equivalent circuit, where the capacitor is responsible to accumulate charge, whereas the resistance and, when present, the inductance are the discharging path. Furthermore, a switch is usually inserted to mimic the *discharge triggering moment* taking place when a charged body gets in contact with a not-charged one. The TLP system used to test the devices in this thesis discussed produces discharges modelled according the *Human Body Model* (HBM)[15]. According the latter, an electronic potential equal to 2 kV or more is connected to a 100 pF capacitor (C_{HBM}), representing the average capacitance of the human body, and a resistance of 1.5 kΩ (R_{HBM}) that represents the average resistance of the human skin (Figure 1-19a)[107]. The discharge trigger is represented by a switch that, upon closure, connects the charged capacitor with a grounded device by means of the discharging path, i.e. the R_{HBM}. A further resistance is inserted in the HBM circuit representing the resistance felt by charges during accumulation periods, virtually infinite, due to the friction with other objects. Such resistance does not take part to the discharging event. The charged capacitor is discharged over the contacted device within few tens of nanoseconds and is characterised by a current reaching values even higher than 10 A. The ESD event modelled by the HBM is thus consisting of a current pulse, potentially destructive for electronic circuits, which imposes the adoption of proper protections. The shape of

such current pulse is depicted in Figure 1-19b. A rise time (t_{ri}) period, of approximately 10 ns, is followed by a discharge time (t_{di}), of approximately 20 ns, during which the current is progressively reduced from the 100% up to 36% of its value[108]. Afterwards, a period of 50 ns follows during which the current is completely nulled. The TLP line I used to test my devices reproduces HBM-like pulses characterised by increasing current amplitude. The TLP produced pulse is squared-shaped, hence not exactly the same as HBM curve shape. Nevertheless, it is designed in such a way to transfer the same quantity of energy a HBM pulse would transfer given a certain maximum current amplitude, therefore the area under the two curves depicted in Figure 1-20a is the same[109]. Such difference is due to the fact that obtaining and reproducing square pulses featuring the same time duration is easier than other type of pulses. In fact, during a TLP test, a train of pulses of the same time length and shape but with increasing amplitude are discharged over the *device under test* (DUT). Figure 1-20b depicts the sequence of increasing pulses a DUT undergoes during a TLP test session[102], [103], [110]. The purpose of such applied train of pulses is to expose DUT to a level of TLP stress progressively higher, in order to find the maximum pulsed energy that it can sustain before suffering permanent damaging.

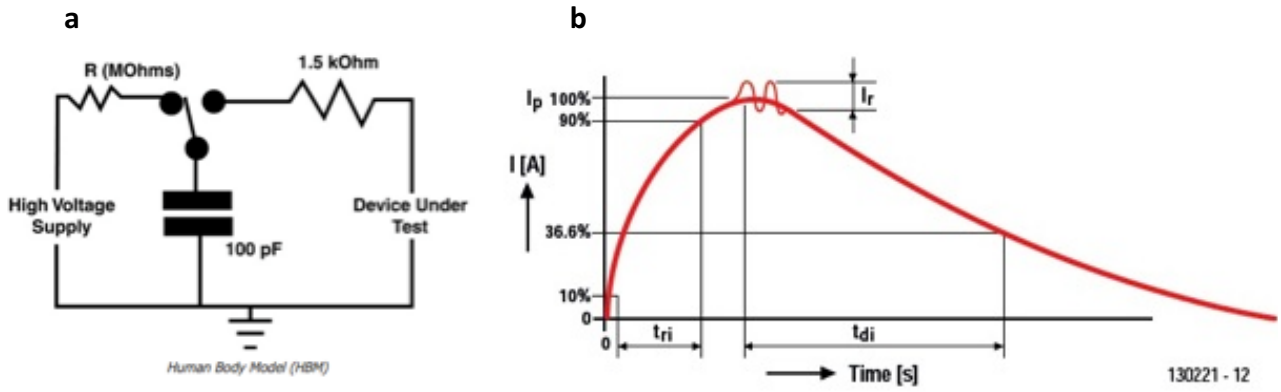


Figure 1-19: (a) The circuit of the human body model (HBM). Adapted from[107]**. (b) The current pulse generated upon an ESD discharge according to the HBM (www.circuitcellar.com).**

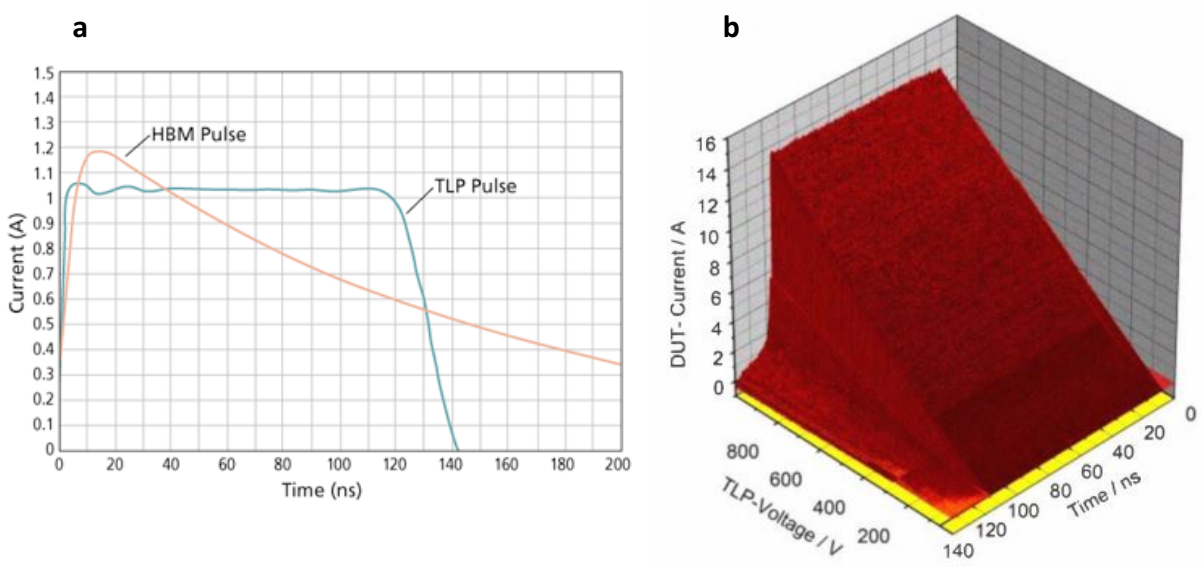


Figure 1-20: a) The modelled HBM pulse and the real applied TLP pulse shape, occurring approximately within 100 ns(www.edn.com) b) The sequence of amplitude-increasing TLP-generated pulses over the DUT. Taken from[110].

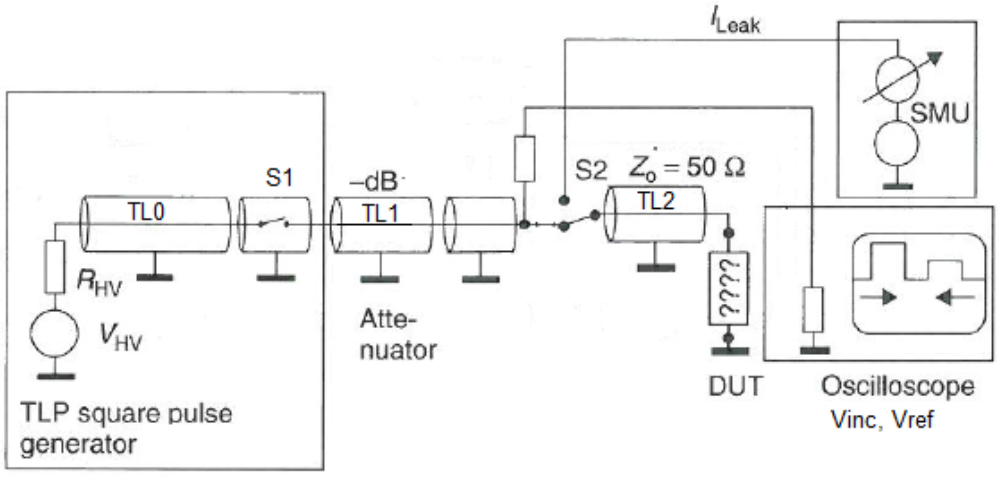


Figure 1-21: A simplified circuit of a TLP line. Adapted from[103].

A summary of the circuit of a TLP system is shown in Figure 1-21[103]. A TLP square pulse generator is connected by means of a switch (S1) to a transmission line (TL1) (a coaxial cable of few meters length) composed by an attenuator and a second switch (S2), responsible to allow the incoming TLP pulse to reach the DUT by means of a second transmission line (TL2) (shorter than TL1). TL0, TL1 and TL2 are characterised by a resistance Z_0, equal to 50 Ω in the circuit proposed in Figure 1-21 (note the TLP system used for the purposes of this thesis features a Z_0 resistance of 200 Ω). S2 is

also used to connect the DUT, between a pulse replica and another, to a source measurement unit (SMU) aimed at assessing the functionality of the DUT during the period in which S1 is left opened. In correspondence of S1 closed and S2 positioned on the TL2, a pulse is released directly over the DUT. The pulse travels through the transmission line to reach the DUT. The pulse is partially reflected back towards TL2, therefore S1 is immediately opened after the pulse release in order to avoid any reflection damaging the pulse generator. The reflection is due to a mismatch between the resistance of the line (Z_0) and the resistance of the DUT. Importantly, the pulse can be reflected back and forth from the DUT to TL2 but, because of the attenuator, the amplitude of such reflections is promptly reduced and negligible rendered. An oscilloscope is connected at the exit of the attenuator in order to detect the applied voltage, also called *pre-charge voltage* (V_{inc}), and the *voltage reflected by the DUT*, called V_{ref}, before the latter reaches the attenuator. V_{inc} is different than the voltage generated by the pulse generator V_{HV} because of the loss due to TL0 and TL1 ($V_{inc}<V_{HV}$). The actual value of the pulse applied across the DUT is termed *TLP voltage* (V_{TLP}), whereas the actual value of current flowing through the device because of the applied pulse is termed *TLP current* (I_{TLP}). V_{TLP} and I_{TLP} can be calculated as:

$$\boldsymbol{I_{TLP} = \frac{V_{inc} - V_{ref}}{Z_0}} \qquad \textbf{Equation 1-12}$$

$$\boldsymbol{V_{TLP} = V_{inc} + V_{ref}} \qquad \textbf{Equation 1-13}$$

The value of these two quantities varies at each pulse replica. The I_{TLP} vs V_{TLP} graphs are fundamental to understand the DUT response to the applied TLP stress and to extract so-called *TLP parameters*, namely the *trigger current* I_{TR}, *the trigger voltage* V_{TR}, the *TLP resistance* R_{TLP} and the *trigger energy* E_{TR}. The I_{TLP} *vs* V_{TLP} is a segmented curve, as shown in Figure 1-22, in which each segment ends in correspondence of a so-called *trigger point*, namely each point in which main changes occur within the DUT so altering its ability to dissipate the pulsed charges. Such changes can be related to various kind of partial damages or total failures, such as arisen short circuits, junction breakdown, and failure of metal contacts. Furthermore, each segment is usually characterised by its own R_{TLP}, or rather the DUT acts as a resistance over which the pulsed I_{TLP} is discharged. As long as the relation between the V_{TLP} and the I_{TLP} is linear this means that the DUT is successfully dissipating the pulsed energy and, expectably, no permanent damages are occurring into the DUT. In correspondence of a trigger point such interdependence between the I_{TLP} and the V_{TLP} changes (red region in Figure 1-22), and therefore suggesting that a permanent damage occurred into the DUT. The value of the

I_{TLP} and of the V_{TLP} corresponding to the trigger point are the V_{TR} and the I_{TR} respectively. The E_{TR} parameter is therefore obtained as:

$$E_{TR} = V_{TR} * I_{TR} * t_{pulse} = P_{TR} * t_{pulse} \qquad \text{Equation 1-14}$$

where t_{pulse} is the duration of the applied pulse by the TLP system on the DUT and the P_{TR} is the trigger power. R_{TLP} can be obtained from the inverse of the slope of the linear segment ending with the trigger point. Each linear segment is characterised by a V_{TR}, an I_{TR}, a R_{TLP} and an E_{TR}. If the latter are referring to segment subsequent to the first trigger point, they are termed as V_{TR2}, I_{TR2}, R_{TLP2}, E_{TR2} or V_{TR3}, I_{TR3}, R_{TLP3}, E_{TR3} etc. Usually, the second trigger point is associated to a permanent failure of the device, and thus, a further exposure of the DUT to TLP stress is avoided by limiting the analysis up to the second trigger point[15]. Furthermore, these parameters can be found in the literature named as V_{t1}, I_{t1}, E_{t1}, R_{on1} or V_{t2}, I_{t2}, E_{t2}, R_{on2}[103], [105]–[107] but, I found less confusing the aforementioned terminology (V_{TR}, E_{TR}, I_{TR}) since in all cases analysed I chose to extract the parameters only up to the first trigger point.

A particular case of TLP parameter extraction takes place when no trigger point is observed, meaning that the device successfully sustained the pulsed energy up to the maximum value the TLP system can supply, i.e. up to the maximum V_{inc}. In correspondence of such case, the parameters are the maximum values observed during the TLP test, therefore they are termed as V_{TLPMax}, I_{TLPMax}, R_{TLPMax} and E_{TLPMax} since no trigger takes place and those parameters are equal to TLP system full-scale.

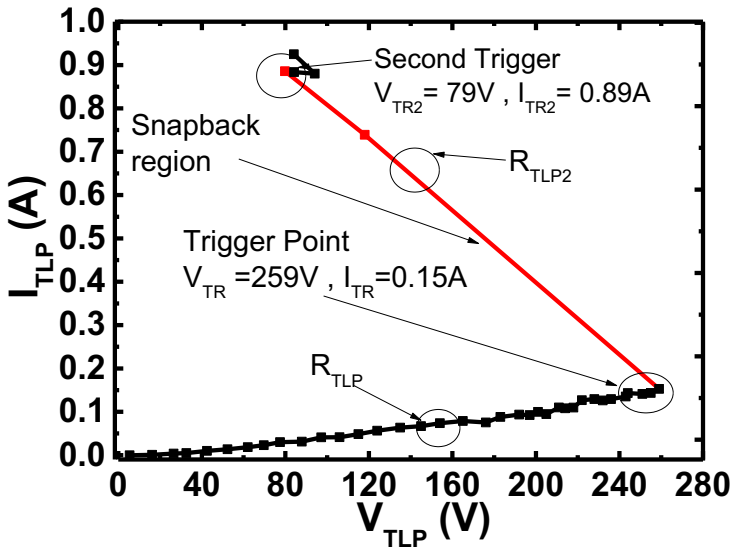


Figure 1-22: The I_{TLP} vs V_{TLP} graph of a PBTTT TLP tested OFET.

The behaviour reported in Figure 1-22 was chosen since representative of almost the totality of cases in the thesis reported. However, the response to TLP stress can be considerably different according the kind of device analysed (single component such as CMOS, FETs or entire integrated circuits) and according the model the TLP system is modelled on (HBM, MM, CMD etc.). An analysis of each of these cases is beyond the purposes of this thesis, which is instead focused only on components tested by means of a TLP set to generate HBM-like pulses. The I_{TLP} vs V_{TLP} graphs measured according such methodology are characterised by: i) a first region of the graph consisting of a straight line; ii) a second region the shape of which depends on the way the DUT dissipates the pulsed energy after the first trigger point. Figure 1-23[106] is reporting two possibilities for ii. The first one (a) shows an increased R_{TLP2} with respect to the R_{TLP} of the first portion of the graph. This happens whenever the dissipated pulsed energy involves a small portion of the device and the DUT resistance is altered in such a way to result less prone to allow pulses to pass through, hence undergoing a considerable heat dissipation leading toward a total failure of the device within few pulses. Such response is similar to a junction breakdown since the accumulated energy is almost fully released after the second trigger point.

The second one (Figure 1-23b) is characterised by a *snapback region*, namely a sudden reduction of the R_{TLP} takes place straight after the first trigger point, so pointing out that the DUT has released part of the accumulated energy in correspondence of the trigger point. The snapback takes place because of arisen parasitic current within the DUT dissipating the pulsed energy and considerably reducing the resistance to the pulsed current[106]. Such situation is generally damaging since the DUT starts working in different conditions with respect to the normal ones, due to arisen parasitic current exploiting electrical paths opened because of both the frequency regime (GHz) the device is forced to work and the physical alterations the dissipated heat induces. A snapback region was observed in almost the totality of the devices in this thesis reported.

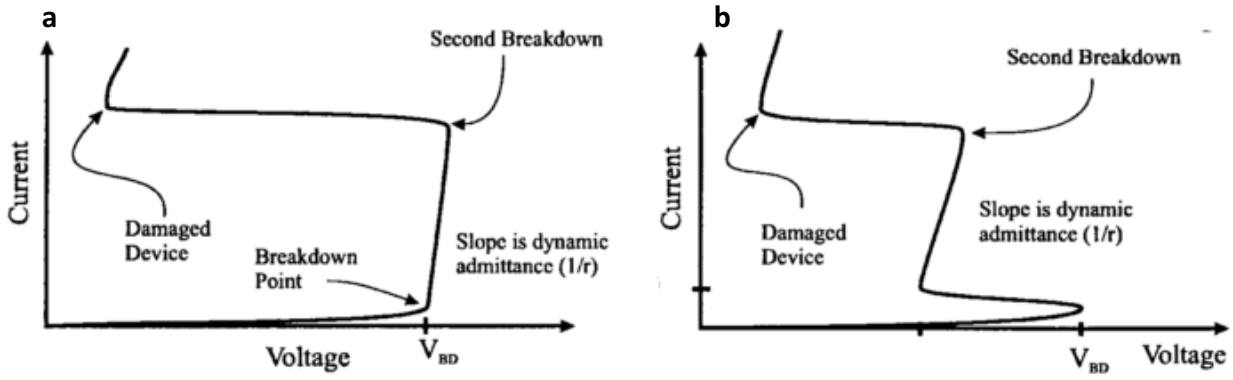


Figure 1-23: Two possible post first trigger point (V_{BD} in the graphs) response to TLP stress by devices undergoing HMB-like pulses: a) junction-breakdown like; b) snapback region. Adapted from[106].

The functionality of the DUT is monitored after each TLP event by measuring the *leakage current* (I_{LEAK}), namely the current flowing through the DUT upon application of a voltage comparable to the operating one. The choice of this parameter corresponds to the selection of the *failure assessment criterion*. In fact, the maximum allowed value for the I_{LEAK} is termed I_{FAIL}. If the I_{LEAK} overcomes such value the so-called *I_{LEAK} test* is failed and it reveals if the applied TLP pulse induces a short-circuit into the device or an abnormally high current flowing through the device in normal operation conditions. Device not failing the I_{LEAK} test are either not experiencing a failure or experiencing a failure of a different kind, such as disruption of electrical connections[111]. Commonly, this parameter turns particularly useful in tests involving a dielectric material, such as gate oxide in field effect transistors, in which ESD events create holes thus inducing short circuits. Furthermore, the I_{LEAK} is normally reported within the I_{TLP} vs I_{LEAK} graph. The shape of such graph gives indications about the DUT in relation of the amount of pulsed current it has been exposed: i) a decrease of the I_{LEAK} for an increasing pulsed current generally indicates a failure of a metal connection internally to the DUT whilst parasitic current, arising solely in the TLP regime, is discharging the pulsed energy via parasitic resistance; ii) sudden fluctuations of the I_{LEAK} and the I_{TLP} itself suggest a failure of the TLP probe-DUT electric contact, as a result of a localised damage over the input pad of the DUT; iii) a steady value of the I_{LEAK} for an arising I_{TLP} is instead indicating that the pulsed current is not causing significant changes in the device; iv) an increasing I_{LEAK} for an increasing I_{TLP} suggests that the TLP pulsed energy is heating the DUT and altering its conductivity, for example by increasing the conductivity of the active layer of organic devices; v) fluctuation of the I_{LEAK} around a certain constant value can suggest the injection of charges that remain trapped into the DUT, especially if

the pulsed current is interesting a dielectric; vi) A sudden increase of the I_{LEAK} is instead revealing a short-circuit. Usually, the I_{TLP} vs I_{LEAK} is a combination of these cases and the passage from a case to another within the same graph can be linked to the passage from a trigger point-limited portion of the I_{TLP} vs V_{TLP} to another. An example of a complete TLP graph, correlated with both the I_{TLP} vs V_{TLP} and the I_{TLP} vs I_{LEAK} (inset) graph in Figure 1-24a is reported.

Another test normally carried out to assess TLP effects on devices is the DC (direct current) test that consists in measuring the device by sweeping a certain set of voltage values. Such test is performed before and after the whole TLP test. The main difference with the I_{LEAK} lies in the latter being assessed at every TLP replica and in correspondence of a unique applied voltage bias, whilst the DC test obtain an entire curve out of the device. For instance, a DC test on TLP OFETs is shown in Figure 1-24b where the curve obtained by sweeping the drain-source voltage between 0 and -40 V and keeping, by means of a third terminal, the gate-source biased at -40 V is measured before and after the TLP test, pointing out an altered behaviour because of the TLP test. Instead the I_{LEAK}, as shown in Figure 1-24a, is measured in correspondence uniquely of an applied V_{GS} of -20 V and an applied V_{DS} of -20 V, there is no sweeping. The DC is therefore aimed at assessing the device functionality immediately after the TLP test.

The parameters obtained by means of TLP tests are used to build ESD protections, in particular the E_{TR} gives an immediate measure of the maximum pulsed energy these devices can sustain, whereas I_{TR} and V_{TR} establish the limit within which the devices must be kept in order to avoid any damage. To obtain this, low-impedance discharging current paths such as Zener diodes, multi-finger gate grounded MOS or metal ring, aimed to shunt ESD currents and clamp the I/O pad voltage to safe levels, are designed accordingly[112]. However, the same TLP parameters can be used also to assess TLP tested devices as ESD protector themselves, since observed low impedance paths arisen upon TLP pulses can potentially be used to deviate pulses from cores of electronic circuits. In such regard, the R_{TLP} is the parameter providing useful information[113].

To the best of my knowledge, only few papers have been reported so far regarding the characterisation of the response of organic FETs[108], [114], as described later, and the work reported specifically for P3HT and PBTTT OFETs[115], [116] is the first one involving these materials, whereas there are no reported papers on OPVs and OLEDs characterised by means of a TLP stressing line.

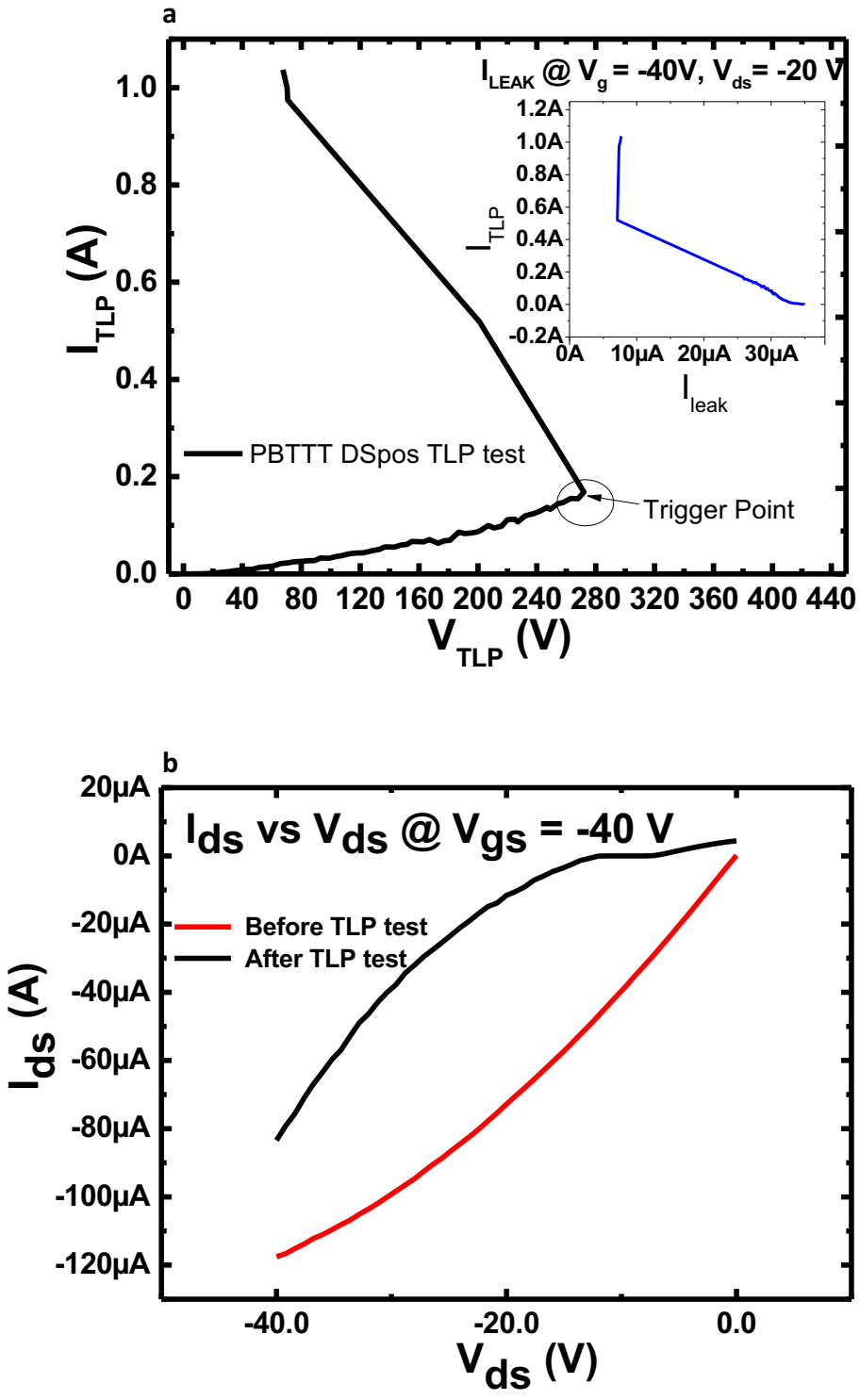


Figure 1-24: A complete TLP graph of a PBTTT OFET tested by applying positive pulses between the drain and the source (a) and the DC test results of the same device before (red line) and after (black line) the TLP test(b).

1.4 Neutron scattering based technique

Neutrons are uncharged particles capable of deeply penetrating into materials so providing information related to the bulk of samples or, by means of fast neutrons, to induce ionisation, recoiling or cleavage into irradiated atoms[17]. Neutrons are scattered by strong and very short (~10-14 nm) nuclear forces, hence neutrons-matter interaction results different compared to X-rays or electrons interactions with matter. For instance, hydrogenated materials poorly deflects X-rays and electrons, whereas they strongly scatter neutrons, and thus, organic materials can be successfully investigated by means of neutron-scattering techniques[22], [117], [118]. Furthermore, the spectrum of neutron energy, obtained within a neutron source, ranges from very low energetic neutrons (0.025 eV) up to highly energetic ones (hundreds of MeV) thanks to a tuning process of neutrons energy (thermalisation) obtained by using a medium at a certain temperature. Such wide spectrum renders neutrons scattering a versatile investigation tool since lower energetic neutrons can be employed for neutron diffraction and spectroscopy, whereas those featuring a higher energy are suitable for damaging tests[10], [119].

1.4.1 Neutrons features

Neutron sources can be of two kinds, namely reactors or pulsed sources. In both cases produced neutrons are far too energetic (> 1 MeV) for spectroscopy purposes, therefore a speed moderating mean is used so as to force neutrons to lose energy via collision to recoiling atoms of the moderator. Emerging neutrons feature an energy content within the Maxwell-Boltzmann distribution of the moderator mean. The moderation can be tuned by changing the mean or its temperature. For instance, if the used mean is water kept at room temperature, the average energy of emerging neutrons is 25 meV, suitable for diffraction experiments, whilst if the mean is liquid hydrogen (<20.28 K) the average neutron energy falls to 5 meV making neutrons suitable for slow inelastic processes or quasi-elastic scattering events[43]. Since temperature affects moderator mean atoms energy, the whole process of neutrons moderation is termed *thermalisation*. Examples of neutrons are: *cold neutrons* with energy ranging between 0.0 and 0.025 eV; *thermal neutrons* featuring an energy of 0.025 eV; *epithermal neutrons* of energy ranging between 10^{-6} to 10^{-1} MeV; *fast neutrons* having an energy ranging from 1 MeV to 20 MeV. Several others can be found featuring different energy intervals such as *cadmium* (kinetic energy below the cadmium cut-off energy, ~0.5 eV), *epicadmium* (kinetic energy between 0.5 eV and 1 eV), *slow* (kinetic energy between 1 eV and

10 eV), *resonance* (kinetic energy between 10 eV and 300 eV) and *intermediate* (kinetic energy between 300 eV and 1 MeV) neutrons.

Neutrons scattering can be elastic or inelastic, depending mainly on neutron speed (cold, thermal or fast) and target nuclei neutron cross section. Neutron cross section is a measure of the likelihood of a neutron to hit a target-nucleus and depends on: i) target type; ii) nuclear reaction; iii) incident particle energy; iv) relative angle between the incident neutron and the target; v) target temperature. Such parameters are therefore to be taken in consideration within the neutron sources in order to tune produced neutrons in such a way to obtain either spectroscopy-suitable or damaging neutrons. An elastic scattering resolves in the total amount of kinetic energy possessed by particles involved, as well as their number, remaining constant after the neutron-sample nuclei collision. According such conditions, no conversion of energy from kinetic into other forms takes place. Elastic scattering is observed in fast neutrons (>1 MeV). Inelastic scattering means instead a transfer of the kinetic energy of the incident particle to the irradiated atoms as thermal energy. Inelastic scattering can activate the target nucleus to an excited unstable state causing a subsequent emission of radiation (alpha, beta, gamma, protons) with the nucleus returning to its ground state. Nucleus can also recoil in other direction. Upon neutron irradiation target materials can experience ionisation, because of direct neutron-nuclei collision involving fast neutrons, or other damages due to inelastic scattering such as recoiling, resonance, cleavage. The latter can take place in CPs upon transfer of an energy from neutrons to nuclei of ~4 eV, or rather the quantity necessary to break a C-H or a C-C bond[10], [22], [119].

1.4.2 **Neutron sources**

Neutrons are obtained either from reactors or pulsed sources. In the first one the neutrons are provided by fission of a fissile material, commonly enriched uranium ^{235}U according the reaction:

$$n + {}^{235}U \rightarrow {}^{236}U \rightarrow {}^{134}Xe + {}^{100}Sr + 2n$$

where n stands for neutron. Such reaction is self-sustaining due to the surplus of neutrons hitting other ^{235}U nuclei and hence renewing the reaction. Neutron scattering experiments in reactor sources require a monochromatic beam necessary to modulate the scattering according to either elastic or inelastic modality. Although the generation of more or less "monochromatic" beams decreases the incident flux, its relatively high initial value counterbalances such degradation[118].

Pulsed sources are obtained starting from a high-energy stream of protons (~ GeV) colliding against a heavy-metal target so as to knock out from the nuclei neutrons and protons. Such process is called spallation[120] and it is based upon accelerator technology. The generated flux is pulsed, differently from the radiation sources in which the flux is steady, and the repetition rate is up to the facility but commonly ranging between 10 Hz and 60 Hz. Generation of monochromatic beams is not required in this neutron source since the common starting point of the neutrons easily permits to determine the associated wavelength λ from the neutron time-of-flight:

$$\boldsymbol{\lambda = \frac{h(t+t_0)}{m_n(L+L_0)}} \qquad \textbf{Equation 1-15}$$

where h is the Planck's constant, t is the time, m_n the mass of neutron, L the total flight path and t_0 and L_0 small calibration offsets. The number of deflected neutrons is normalised against the distribution of the beam measured using a neutron monitor after the moderator before using the beam over the sample.

Importantly, pulsed sources have become increasingly popular among scientist and are relatively easier to set up because do not rely on fissile material, also posing less political/social issues. The experiments involving neutron irradiation reported in this thesis were carried out in the neutron pulsed facility within the Rutherford Appleton Laboratory, ISIS, in Oxfordshire (U.K.) that operates at 160 kW and characterised by a flux repetition rate of 50 Hz in the target station 1 (VESUVIO), where my samples were irradiated.

1.4.3 **Neutron Irradiation**

Neutrons are exploited mostly for: i) *neutron reflectivity*, namely a diffraction technique useful to measure sample thickness, roughness and chemical composition; ii) so-called *quasi-elastic neutron scattering (QENS)* spectroscopy; iii) *neutron irradiation* to mimic the exposure to secondary neutrons that instruments experience in aircrafts and spacecraft. Techniques i and ii were not used for the purposes of this thesis, whereas technique iii was used on OFETs and OPVs, as reported in chapter 4. In fact, my purpose is to quantify the loss of figures affecting photovoltaic cells because of the prolonged interaction with neutrons, namely years of utilisation in space. Devices exposed to neutrons for periods of few hours according technique iii receive a dose of neutrons equivalent to the dose they would receive staying years in space. Such condition is ideal to assess neutron exposition long-term effects on devices. Neutron exposition can also be termed *neutron hardening* whereas the period of time during which devices or samples are exposed to neutron irradiation are

termed *aging periods*. Techniques i and ii do not provide a sufficient level of neutrons to achieve such accelerated stressing condition.

Although QENS technique was not used within the work carried out for this thesis, few words are worth to be said since such technique is particularly interesting for the analysis of CPs. In fact, QENS is obtained by using neutrons characterised by an energy close to the elastic limit, hence in a regime where a small portion of neutron kinetic energy is converted into thermal energy to the target nuclei. In such conditions, neutrons interact with target nuclei and are sensitive to phenomena characterised by timescales ranging between 10^{-13} s and 10^{-9} s and lengths of 1 to 30 Å, therefore sensitive to polymer segmental motions, translation or rotation that take place within the QENS detection capabilities[119].

Neutron irradiation is a well-established technique to mimic the effects of cosmic rays on silicon-based electronics for space and avionics applications. In fact, due to cosmic rays interaction with structural shielding of spacecraft, highly energetic stream of secondary neutrons can be generated and, therefore, equipment and crew on board are constantly exposed to this stream. Cosmic rays are generated outside the solar system and are composed for the 90% by protons and for 10% by ionised atoms. Secondary neutrons are also generated from interaction of cosmic rays with atmosphere. In fact, neutron irradiation normally takes place at different altitudes because of atmospheric neutrons. To assess the long-term effects of such neutron irradiation on equipment and materials so-called neutron irradiation technique is carried out within neutron sources, since these provide an intense fast neutrons flux.

In this thesis, I analysed neutrons irradiated OFETs and OPVs according different neutron aging periods. For our irradiation experiment (chapter 4), I took advantage of the VESUVIO beamline at ISIS - Neutron and Muon source. VESUVIO beamline is mainly a neutron spectroscopy beamline but, by tuning the moderation of the neutron beam, a flux of neutrons featuring an energy spanning from meV to MeV can be obtained so permitting neutron aging tests too[120], [121].

2. Material and methods

In this chapter, the first section describes the materials used (P3HT, PBTTT, PCBM , F8BT). Section two, three and four introduce the fabrication procedure and the electrical characterisation of OPVS, OLEDs and OFETs respectively. The fifth section briefly describes the optical investigation technique used to analyse TLP stressed devices, namely photoluminescence and Raman spectroscopy. The TLP characterisation of OPVs, OFETs and OLEDs is described in the sixth section. Finally, neutron irradiation energy spectrum used for OPVs and OFETs neutron hardening is introduced in the last section.

2.1 P3HT, PCBM, PBTTT and F8BT

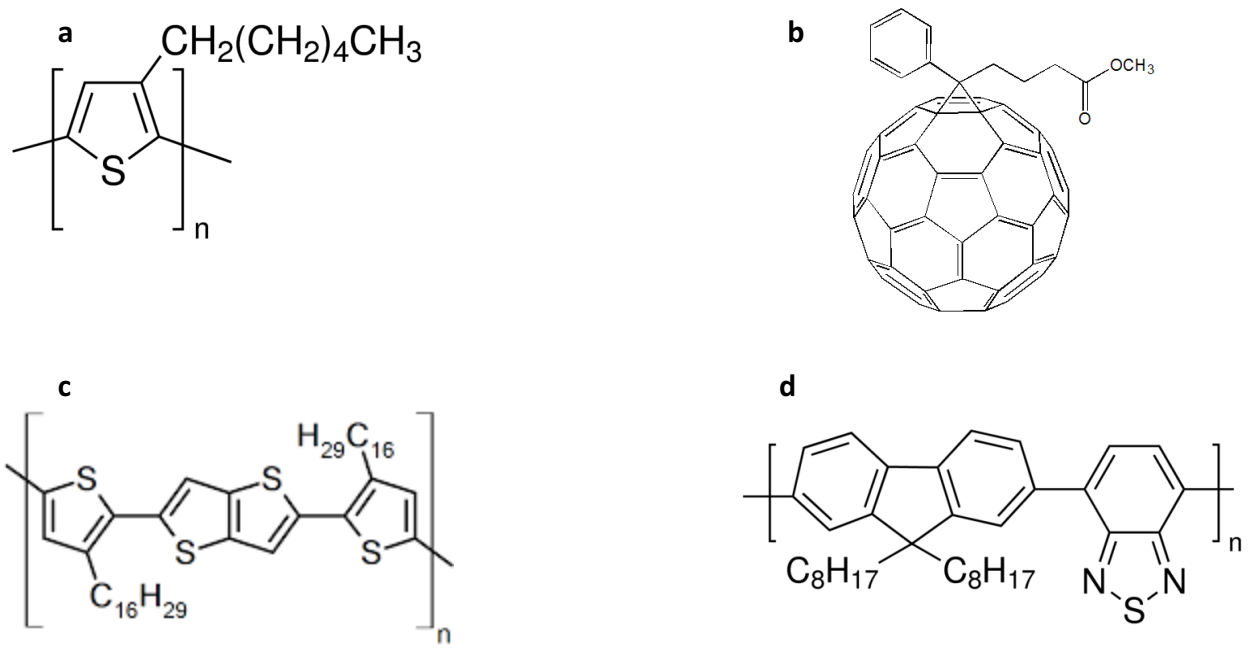


Figure 2-1: the chemical structures of: a) P3HT;b)PCBM; c)PBTTT; d) F8BT.

Regioregular Poly(3-hexylthiophene) (P3HT) (Figure 2-1a) is a semiconducting polymer largely used in organic electronics primarily because of its regular end-to-end arrangement of side chain, yielding an efficient p- p stacking of the conjugated backbones[68], [122]. P3HT it is used as active layer of OFETs and also blended with [6,6]-Phenyl-C61-butyric acid methyl ester (PCBM) in bulk heterojunction solar cells. P3HT features a HOMO level of 5 eV and a LUMO level of 3 eV and it

features a hole mobility of ~10^{-4} -10^{-2} cm^2/Vs, and approximately a tenfold lower electron mobility[51], [96], [123], [124].

PCBM (Figure 2-1b), instead, is a solubilised version of the buckminsterfullerene, C60, and it is well known as one of the most commonly used electron accepting materials in organic photovoltaic devices. When blended with other donor materials, such as P3HT, it enables an efficient charge transfer and exciton dissociation[125]. PCBM features a HOMO level of 6.1 eV and a LUMO level of 3.7 eV, whereas the electron mobility is approximately of 10^{-3} cm^2/Vs.

Poly(2,5-bis(3-hexadecylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT) (Figure 2-1c) is usually used to be blended with fullerenes since its structure features adjacent side-groups that are positioned sufficiently far apart so that they can permit the molecular intercalation of these[12], [96]. The microstructure of PBTTT is similar to the lamellar organization of P3HT but the lower density of side chains in thiophene-thienothiophene copolymers increases the ionization potential, improves the stability, allows a better side chain interdigitation resulting in a highly crystalline structures[41]. Such properties render PBTTT higher conductive than P3HT. PBTTT features a HOMO level of 5.1 eV, a LUMO level of 3.1 eV and a hole mobility of ~1 cm^2/Vs.

Poly(9,9-dioctylfluorene-alt-benzothiadiazole) (F8BT) (Figure 2-1d) is a largely used CP as active layer in OLEDs, as a quasi-balanced p-type and n-type semiconductor for OFETs and as active layer in light emitting transistors. It can also be used as polymeric acceptor for OPVs. F8BT is a green emitter (~550 nm) featuring a HOMO/LUMO levels of 5.9 eV/3.3 eV and hole mobility of ~$4x10^{-3}$ cm^2/Vs[126]–[129].

The fabrication process of the devices in this thesis reported exploited the utilisation of thin films obtained out of the materials previously mentioned. The thickness of these films has been measured by means of the instrument Dektak 3 Surface Profilometer and optimised by accordingly tuning the rpm used during the spin-coating process.

2.2 Solar cells fabrication and characterisation

I prepared P3HT:PCBM bulk heterojunction solar cells by using OSSILA substrates (8 pixels- 4.5 mm^2 active area) suitable for encapsulation, which were cleaned in a sonication bath of 10 minutes in isopropanol and in a second one of 10 minutes in acetone. An oxygen plasma treatment of 10 minutes was carried out in order to increase the wettability of such substrates. Afterwards, I spun-coated in air Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS) onto

these devices (5000 rpm – 60 s resulting in a 40-50 nm thick layer) and I carried out a thermal annealing at 100° C for 10 minutes in glovebox (inert environment). A solution of P3HT and one of PCBM, both in chlorobenzene according to a concentration of 20 mg/ml, were prepared and, after a stirring period of 12 hours, filtered by using a 10 µm diameter pores polytetrafluoroethylene (PTFE) filter. Eventually, the two solutions were mixed according to a ratio of 0.7:1 in volume and the resulting solution was left in stirring for 12 hours prior its utilisation as active layer in the cells. I spun coated this solution onto the substrates, prior treated as reported above, in glovebox (1600 rpm for 60 s + 4000 rpm for 10 s resulting in a 180-200 nm thick layer). An annealing of 10 minutes at 100° C in glovebox was carried out on the substrates spun with the active layer before undergoing the evaporation process of the cathode, namely a 30 nm-thick calcium layer and a 100 nm-thick aluminium layer. After the evaporation, the devices were encapsulated by using glass slides glued over the bottom side of the devices, above the aluminium layer, by means of an UV-strengthen epoxy. The structure of the cell and the energy bands diagram of the material involved are respectively reported in Figure 2-2a and Figure 2-2b.

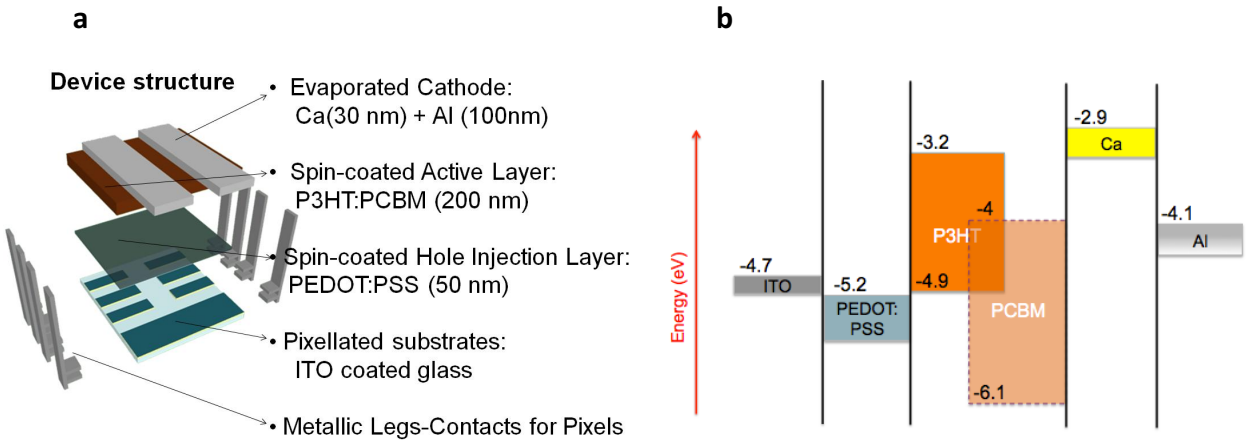


Figure 2-2: a) The structure of the solar cells obtained by using the OSSILA substrates. These devices are provided of 8 pixels that feature an active area of 4.5 mm². b) The band diagram of the material involved into the P3HT:PCBM BHJ cells.

2.2.1 Solar cells electrical characterisation

I characterised the solar cells by means of an AAA class Sun 3000 11016A ABET Sun simulator and of a Keithley 2100. Solar cells were impinged by a light intensity of 1 Sun (1000 W/m^2) and JV curves were measured by applying a voltage spanning from -0.2 V to 1 V between the anode and the cathode. I measured both the dark current and the current generated under illumination. For the

in-operando illumination during the neutron hardening tests and the TLP tests, I used a tungsten halogen LS-1-CAL Ocean Optics lamp which was providing a light intensity of 0.8 Sun (800 W/m^2).

2.3 Organic transistors fabrication and characterisation

Regioregular P3HT purchased from Sigma Aldrich and PBTTT purchased from Ossila Ltd were used to build the OFETs used in the research activity here reported. P3HT solution is dissolved in chlorobenzene at room temperature (RT) with a concentration of 10 mg/ml, whereas PBTTT is dissolved in 1,2 dichlorobenzene at 80°C. Both solutions are then filtered by using a PTFE syringe-filter with 0.20 µm (diameter) pores. Bottom-gate/bottom-contact transistors are then prepared by spin-coating these solutions on silicon/silicon oxide substrates, featuring pre-patterned Au source and drain electrodes. Importantly, as PBTTT is soluble in chlorinated solvents for a temperature above 70 °C, to prevent formation of a defect-rich interface induced by the quick crystallization of the solution upon contacting the cooler substrate, both the PBTTT solution and the substrates are kept at the same temperature (~80 °C) before spin-coating. This procedure is not required for P3HT.

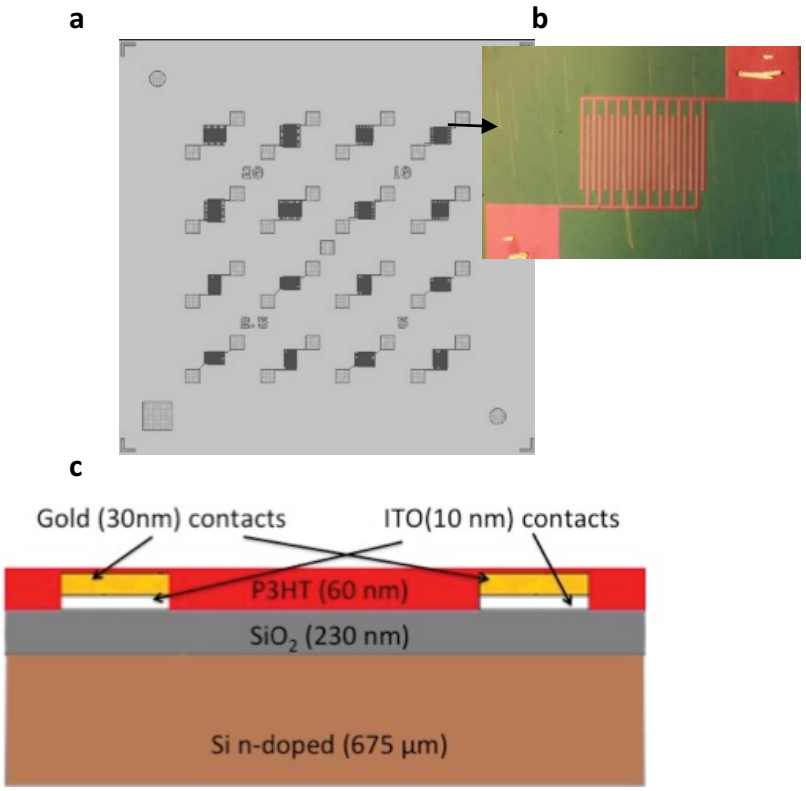


Figure 2-3: Top-view of the Fraunhofer IPMS OFETs substrate (15 mm x 15 mm) (a), of a single 10 µm channel length transistor (b) and of the cross section of a single film transistor (c) obtained via deposition of P3HT onto the interdigitated substrates. Transistors are organised according to their channel length.

The substrates used were purchased from Fraunhofer Institute for Photonic Microsystems (IPMS). On each substrate 16 transistors, with four different channel lengths (2.5 µm, 5 µm, 10 µm and 20 µm) are located on top. All transistors have a channel width of 10 mm and a common gate contact located on the bottom of the chip. Substrates are composed by a 675 µm n-doped silicon bottom layer, acting as bottom gate, capped with a 230 nm SiO_2 layer that is in turn patterned with interdigitated metal lines and pads, the latter acting as source and drain contacts. Metal lines are obtained out of a 30 nm Au layer. Au adhesion to substrates is increased by using a 10 nm ITO layer laying in between the SiO_2 and the Au layers. The structure of the entire chip, of a single transistor and of the cross section of one of the transistors are shown in Figure 2-3.

For the preparation of these devices the first step is an oxygen plasma treatment of OFET substrates. Afterwards, a hexamethyldisilazane (HMDS) layer is spin-coated over the samples that are subsequently annealed at 100° C for 1 h. HDMS is an organosilicon compound that has been shown to improve the mobility of p-type OFETs[51] by favouring active layer crystallisation. After the annealing, substrates are spin-washed with isopropyl alcohol (in glove-box) before undergoing another thermal annealing at 100° C for 10 minutes aimed at removing HMDS in excess so obtaining a very thin layer (~5nm) of the same. HMDS was purchased from Sigma Aldrich. At this point of the preparation substrates are ready to be coated with organic active layers. Both P3HT and PBTTT layers are deposited via spin-coating and, once spun, another thermal annealing at 100° C for 10 minutes is carried out to help residual solvent, used for the preparation of P3HT and PBTTT, to evaporate. The cross-section of a P3HT transistor (equivalent to PBTTT ones) is presented in Figure 2-3c. These OFETs are three-terminal devices with no bulk-terminal. Once spun, P3HT and PBTTT form the semiconducting channel of the transistors. The active layer thickness is between 60 and 70 nm. I did not apply any passivation on the uppermost layer (active layer and drain-source terminals) in order to allow a direct access on the terminals of the devices and to permit Raman spectroscopy analysis of the chips prior and after the TLP stress.

2.3.1 OFETs electrical characterisation

P3HT and PBTTT display higher hole-mobility than electron mobility, therefore they are best suited for p-type (accumulation) OFETs, and this is the operation mode I used in my experiments. First, I carried out a preliminary characterisation of the devices by recording the transfer and output characteristics (at room temperature) by means of a PM5 Cascade-Microtech wafer prober and a HP 4145B semiconductor parameter analyser. The output characteristics of transistors have been

obtained by sweeping the gate-source voltage (V_{GS}) between 0 V and -80 V and the drain-source voltage (V_{DS}) between 0 V and -80 V. The transfer characteristics have been obtained by sweeping the V_{GS} between 10 V and -80 V for and applied V_{DS} of -20 V and -80 V. In order to obtain the mobility from the equation 1.10, the value of C_i was calculated by using the vacuum permittivity (ε_0=8.854x10^{-12} F/m) times the relative permittivity of silicon oxide (3.9) split by the oxide thickness (230 nm), hence resulting C_i = 1.5x10^{-4} F/m^2[130].

2.4 Organic light-emitting diodes (OLEDs) fabrication preparation and electrical characterisation procedures

F8BT purchased from Ossila Ltd was used to build F8BT OLEDs. F8BT is dissolved in toluene according 2% in weight per ml. The so prepared solution is then kept in stirring for 2 hours at 360 rpm and at 60°C. The solution is filtered before spin-coating by using a PTFE filter (0.20 µm pores diameter). Spin-coating is performed at 1800 rpm for 120 s and an approximately 100 nm thick layer is obtained. The substrates used are the same described in section 2.2 and the PEDOT:PSS coating procedure is also the same. The resulting structure is equivalent to the one shown in Figure 2-2a, except for the active layer that, in this case, is F8BT. In Figure 2-4 it is possible to see a F8BT OLED working.

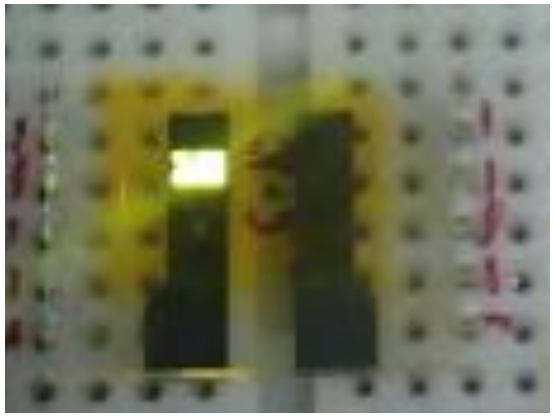


Figure 2-4: One of the F8BT encapsulated OLED used for the studies in this thesis reported. The picture was taken by means of a 13 Megapixel CCD camera with a f/2.0 lens, optical zoom 2x.

OLEDs electrical characterisation

The current density and luminance versus voltage (JLV) characteristics are measured with a Keithley 2004 source-meter and a calibrated Si photodiode coupled to a Keithley 2000 multimeter. A Si

photodiode, with an area of 100 mm^2, detects photons emitted by the device (the emitting device area is 4.5 mm^2, i.e. a pixel area). The light output intensity is directly proportional to the current flowing through the LED. The emission intensity versus wavelength, i.e. the EL spectrum, is measured by using an ANDOR-Shamrock spectrograph coupled with an ANDOR-Newton charge-coupled device (CCD) unit.

2.5 TLP devices characterisation

The TLP measurements of the devices, which are presented in this thesis, are tested by means of a home-built Transmission-Line Pulsing system (TLP) at the Analysis and Test of Integrated Systems (ATIS) group in Fraunhofer research institution for microsystems and solid-state technologies (EMFT), at room temperature. This characterisation provides the component behaviour during an ESD event without the self-heating issue of standard IV measurements[14], [103]. This test uses short square pulses in the time-domain according to the Human Body Model (HBM) electrostatic discharge. The rise time of the applied TLP pulse provide information on the ability of the device under test (DUT) to trigger correctly when an ESD pulse is applied. The width of the applied pulse indicates the energy the DUT has to sustain during an ESD event. The system used is a constant current TLP provided with an impedance (Z_0) of 200 Ω, whereas the pulses used in the tests are, on average, 100 ns wide including a 5 ns rise time and 5 ns descending time. The mean value of the pulse duration is also given by the system in order to correctly obtain the value of the pulsed energy. Calibration steps were carried out on the system to prevent all systematic errors due to cables, connectors, oscilloscope and temperature with open-short correction circuits and a standard Zener diode. Per each device the TLP parameters are obtained by directly analysing the I_{TLP} vs V_{TLP} graphs and the I_{TLP} vs I_{LEAK} values. The time passing between one pulse to another is ~1 s, during which the I_{LEAK} is obtained[15], [116]. After each test, also the DC curves were measured. A TLP test is characterised by the polarity of applied pulses and by a bias a third terminal can apply over the devices. By combining these last two factors several possible TLP test setups can be obtained. The chosen TLP setups per each test are described in the following chapters.

2.6 Optical Characterisation

2.6.1 PL and absorption spectra

The photoluminescence spectra (PL) were collected with an Andor Shamrock spectrograph (spectral resolution of 1 nm) coupled with a charge coupled device (CCD) camera. The PL measurements were

conducted exciting the samples with a 450 nm wavelength diode laser. The absorption measurements were obtained using an Agilent 8453 spectrophotometer with spin-coated 200 nm thick films of P3HT-PCBM blend over fused silica ("Spectrosil") substrates. The latter were spin-coated with a 40 nm layer of PEDOT:PSS prior the P3HT:PCBM deposition.

2.6.2 **Raman Spectra**

In Raman Spectroscopy photons of a single wavelength, generally obtained by using a laser, are focused onto a sample. Such photons can be reflected, adsorbed or scattered. The latter are mostly *elastically* scattered, therefore maintaining the same wavelength of incident light. Such scattering is called *Rayleigh scattering*. However, approximately 1 out of a million photons are *inelastically* scattered, as first described by Sir Chandrasekhara Raman in 1922[131]. Raman spectroscopy draws upon inelastically light scattering that is directly revealing information on vibrational modes of the molecules, and therefore about the vibrational spectrum for the identification of molecules and their functional groups[83], [132], [133]. According such phenomenon a photon is scattered inelastically by a crystal with the creation or annihilation of a phonon or magnon[134]. The process is identical to the inelastical scattering of x-rays and analogous to the inelastic scattering of neutrons by a crystal.

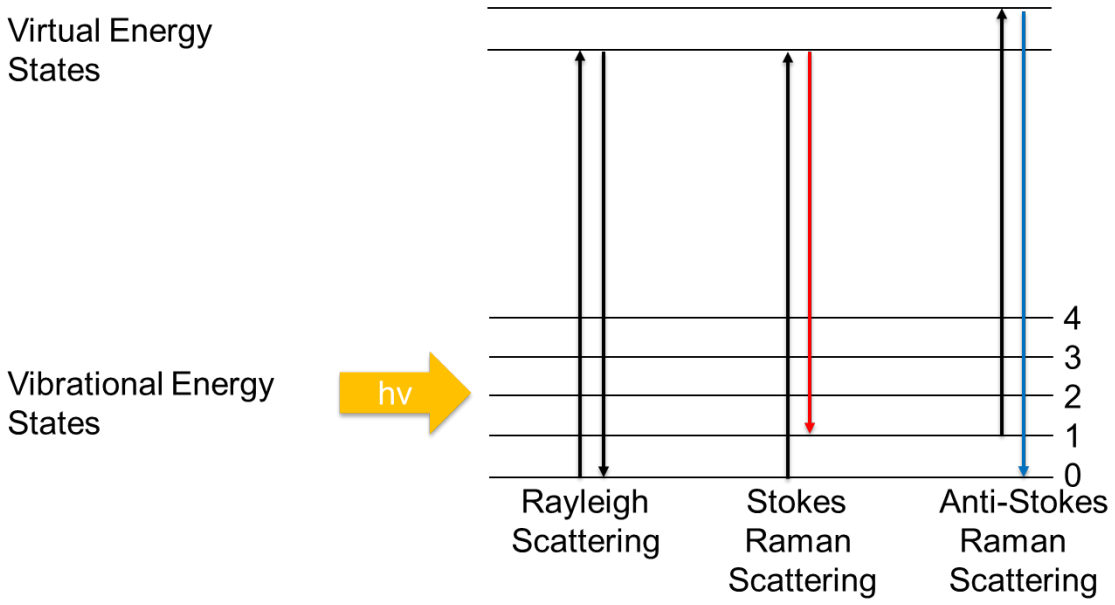


Figure 2-5: Upon light (hν) beamed over a sample, photons can undergo Rayleigh, Stokes Raman or Anti-Stokes Raman scattering.

For an incident photon interacting with matter its wavelength can be either shifted lower (red shift), and hence undergo a so-called *Stokes shift*, or shifted higher (blue shift), and hence undergo so-called *Anti-Stokes shift* (Figure 2-5). In Stokes shifts, photon interact with electron cloud of the functional group bonds exciting these into a virtual state. Therefore, photon transfer a portion of their energy to these electrons, which in turn are excited and moved into a virtual state (vibrational modes) to subsequently relax into a vibrational state. The portion of energy lost by photons is directly depending on the functional groups, atomic bonds or the molecular structure the photon interacted with. The polarisation state of the molecule and its change caused by the interaction with light is directly influencing the so-called *Raman scattering intensity*, the more the functional group are polarised the more their Raman scattering is intense, therefore not all vibrational or rotational transitions are *Raman active*[135].

The Raman Spectrum is hence characterised by the intensity of the Raman signal on the Y axe, generally normalised with respect to the highest of the peaks found in the spectrum, whilst it is characterised by so-called Raman Shift on the x axe, namely a wavenumber expressed in cm^{-1} and defined as:

$$\boldsymbol{Raman\ Shift} = \frac{\mathbf{1}}{\boldsymbol{\lambda_0}} + \frac{\mathbf{1}}{\boldsymbol{\lambda_1}} \qquad \textbf{Equation 2-1}$$

where λ_0 is the wavelength of the incident light whilst λ_1 is the Raman spectrum wavelength. A Raman micro-spectrometer is a Raman spectrometer exploiting one or more lasers, of different wavelengths, integrated with an optical microscope. Raman spectra are acquired by beaming one of the laser on the sample onto an area of few microns of diameter[136]. Raman spectroscopy exploiting lasers characterised by a wavelength causing electrons to jump into excited states, and so generating PL phenomena, is working in so-called *resonant conditions*, whilst in *not-resonant conditions* in other cases[137].

The OFETs reported in chapters 3 and chapters 4 were analysed by means of a Renishaw inVia Raman microscope (50× objective) with an excitation wavelength of 785 nm (non-resonant conditions). The laser power was set at 1% of its maximum power to avoid photo-degradation of the sample (1 – 5 mW). The spectra were taken at room temperature in the Stokes' region and were calibrated against the 520.5 cm^{-1} line of an internal silicon wafer. The signal-to-noise ratio was enhanced by repeated acquisitions. Spectra were corrected by subtracting the samples fluorescence background affecting the spectra baseline by using the "peak analyser" tool within OriginPro 9

program. The baseline to subtract is obtained by means of a b-spline interpolation of spots manually chosen over each spectrum. The Raman spectra were collected from each of the tested devices and compared with a reference spectrum taken from a pristine device, built within the same fabrication session of the tested one and according the same procedure and by using the very same materials. I could not carry on any Raman analysis on OPVs or OLEDs because of the encapsulation not permitting to directly beam the exciting laser over the pixels, whilst only strong fluorescence signal was obtained by trying to reach the polymer beaming the laser through the silica composing the OSSILA substrates used to build encapsulated devices.

2.7 Neutron aging exposure

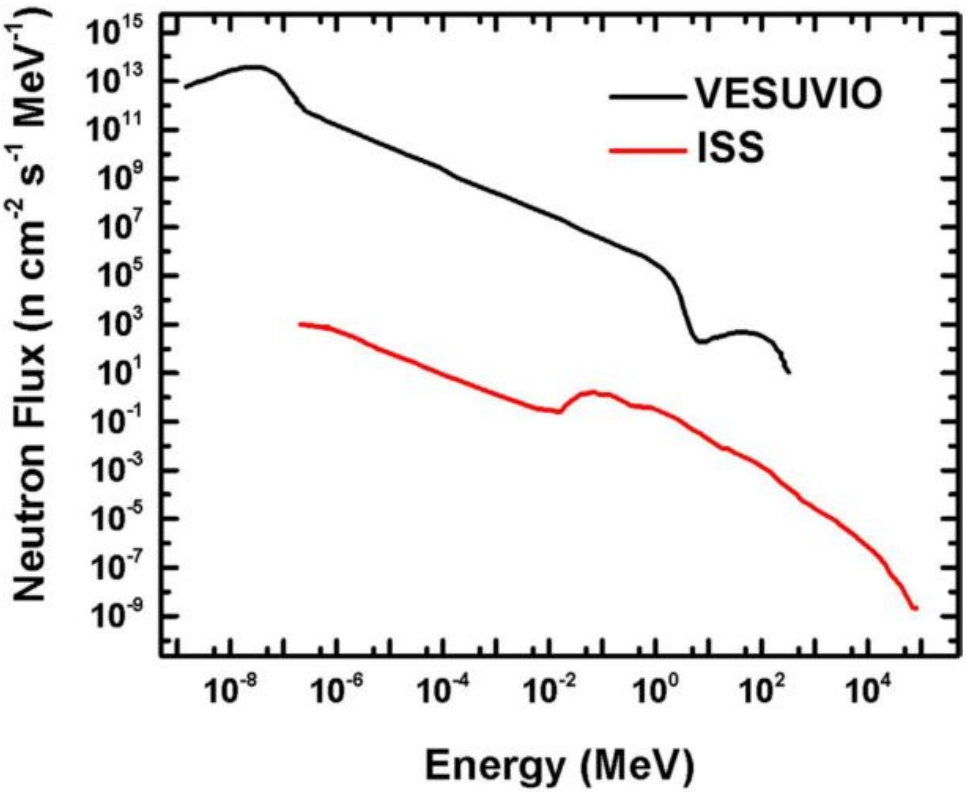


Figure 2-6: The energy profile of neutron flux in the VESUVIO beamline and in the ISS. Taken from[10].

The experiments involving neutron hardening in this thesis reported were carried out at the VESUVIO beamline within the RAL laboratories. In Figure 2-6 the energy profile produced within such beamline[138] is reported and compared to the one measure on board the ISS[139]. The spectrum results pretty broad in both cases but VESUVIO-spectrum shows higher level of neutron flux, and thus, indicating that the neutron irradiation experiments within such beamline can be used to mimic an accelerated exposure to neutrons of devices on ISS. In particular, the number of

epithermal-neutrons (10^{-6} to 10^{-1} MeV) generated within VESUVIO is resulting up to seven orders higher than those registered within the ISS. Taking in account only fast neutrons with energy higher than 10 MeV, which flux value in the VESUVIO beamline is 5.82×10^4 n cm^{-2} s^{-1}, Paternò et al.[10] estimated that samples exposed to such flux absorb in six minutes the equivalent neutrons quantity of 1 year of irradiation on the ISS, hence in 1 hour the equivalent of 10 years. Such accelerated exposure rate can be assumed valid for the samples reported in this thesis as well.

3. TLP Experimental Results

Organic semiconductors have attracted great interest due to their easy manufacturing[31], low cost requirements and suitability for flexible and stretchable devices. In particular organic light-emitting diodes (OLEDs), organic photovoltaics (OPVs) and organic field-effect transistors (OFETs)[7], [42], [140]–[142] have been beneficiating of these materials, and thus extensively studied and constantly improved, resulting particularly appealing for a wide range of applications such as artificial electric skin for robots[143], [144], prosthetics[145], energy harvesting[146], [147] and space[47].

OPVs, for instance, can be embedded in home curtains and windows or used to cover spacecraft and aircraft externally. These utilisations require flexible mechanical properties and low production costs, therefore the properties featured by organic materials could act as key factor to replace inorganic ones[148], [149]. However, a large spread of these devices is yet to take place since researchers have to address and solve problems related to organic devices performance in comparison of those inorganic devices provide.

Some of the aspects addressed to close the gap between organic and inorganic devices are: (i) enhance the power conversion efficiency (η) of OPVs, the best reported organic solar cell η is 12.6%[150] whilst inorganic ones range from 21.2 % (thin film crystal silicon cells) to a maximum of 28.8 % (thin film crystals of GaAs)[12], [151]; (ii) long-term reliability and durability[4], higher in inorganic; (iii) lack of a reliable response to the mechanical fatigue[152]–[154]; (iv) lower charge mobility and higher activation bias required for V_{TH} of transistors and V_{on} of OLEDs (up to tens of volts) in comparison of values required for inorganic devices (~1 V or lower); (v) long term electrical reliability[108], [114], [116]. Whilst points (i)-(iv), are largely discussed and matter of many reported works, point (v) encompasses a study poorly covered so far in literature, namely the characterisation of the response of organic devices to electrostatic discharge (ESD) phenomena. This is particularly relevant since ESD events are likely to affect devices throughout their lifetime and lead to devices failure therefore imposing appropriate protections[23]. The latter, in turns, are specifically designed on the basis of TLP tests[102], [103]. Several papers on inorganic-based circuits characterised via TLP are reported in literature[100], [101], [106]. On the contrary, the characterisation of the robustness of organic devices to ESD events, to date, has scarcely been considered in literature,

even though it could definitely pave the route towards a large spread of OPVs as well as OLEDs and OFETs.

The few works so far reported on organic devices TLP-tested are focused on OFETs or single layers used to build organic devices, i.e. PEDOT:PSS. Bonfert et al published papers on flexible PEDOT:PSS 3 µm-thick films tested by means of a TLP line[110], [155], [156] set in the Time Domain Reflection (TDR) regime and applying pulses 100 ns long. They observed PEDOT:PSS films can sustain TLP pulses up to a pre-charge amplitude of 300 V without suffering permanent damages, above which overheating causes fatal damages. Bonfert also observed that by adding 6 % in volume of ethylene glycol (EG) to the PEDOT:PPS solution the films subsequently featured an increased robustness to TLP stress, resulting damaged for a pre-charge amplitude over 380 V. Liu et al. analysed the failure mechanism due to ESD events in pentacene OFETs[108], [114]. They observed the rupture of the drain contact upon failure of the stressed devices. The highest current these devices withstand is 0.468 A, occurring for an applied voltage of 702 V. Furthermore, by applying a bias on the gate of TLP stressed devices they found a correlation between TLP-discharges and the parameters trigger voltage, failure current and resistance to failure. In two previous papers we reported for the first time about the response of regioregular poly (3-hexylthiophene-2,5-diyl) (P3HT) OFETs upon 100 ns wide TLP applied pulses[115], [116]. We directly involved the organic semiconductor by applying positive pulses between the drain and the source of the devices finding out a correlation between the channel length and the trigger voltage. A maximum 315 V voltage trigger was registered for a 20 µm length channel and corresponding to a trigger current of 0.2 A. Three different channel lengths were investigated, i.e. 20 µm, 10 µm and 5 µm. We also analysed the robustness of the 250 µm-thick silicon oxide gate of these devices measuring a failure current of 0.09 A corresponding to a trigger voltage of 315 V. We finally analysed how the I-V curves, the threshold voltage and the charge carrier mobility changed according to the dissipated power between the drain and the source, which results significantly damaging for the interdigitated drain and source metal lines. The results published in[115], [116] are inserted within the larger investigation reported in section 3.2.

In the first section of this chapter I report on the effects of the TLP stress on the JV curves and the photovoltaic parameters of P3HT:PCBM BHJ solar cells. I analyse the different responses in the case of negative and positive applied pulses and also how these vary in case such pulses occur whilst the cells are under illumination or not and biased with an anode-cathode (V_{AC}) voltage. Hence, I analyse the photovoltaics parameters of the cells that did not fail during the test and the photoluminescence of all the samples tested. I also describe the cells behaviour according to the equivalent electronic

circuit of solar cells pointing out the role of the series resistance (R_S) and the shunt resistance (R_{SH}). Notably, this work, at the best of my knowledge, is the first work carried out on OPVs tested by means of a TLP system.

In the second section of the chapter I analyse the response to TLP stress of P3HT and PBTTT OFETs. The tests were carried out by employing both negative and positive pulses in correspondence of different bias values for the V_{GS}. TLP parameters in each case-study are obtained and, in those cases the OFETs resulted still functioning after the TLP test, a characterisation of the electric parameters (V_{TH}, μ, on/off) of TLP-stressed OFETs is also reported. Raman spectroscopy of TLP-stressed devices is also reported.

In the third section, the results of OLEDs tested by means of TLP are reported. I tested OLEDs according different V_{AC} bias values and pulse polarities. TLP parameters obtained in each case studied and, in those cases OLEDs managed to sustain up to the maximum V_{inc} of the TLP system, JVL and LV curves of OLEDs before and after TLP stress are reported.

3.1 TLP test on P3HT:PCBM OPVs

I carried out four different TLP tests by applying positive and negative TLP-pulses between the anode and the cathode of the OPVs in both illumination and dark conditions: (i) positive TLP in dark conditions, (ii) positive TLP under illumination, (iii) negative TLP in dark conditions, (iv) negative TLP under illumination. Each of the aforementioned tests was repeated on three different pixels, and thus the average values and the corresponding variance were calculated accordingly. Each graph here reported is representative for all the pixels treated in the same TLP-conditions. Devices are built and tested according procedure described in 2.2. PL investigations are carried out as described in 2.6.1.

3.1.1 TLP test results

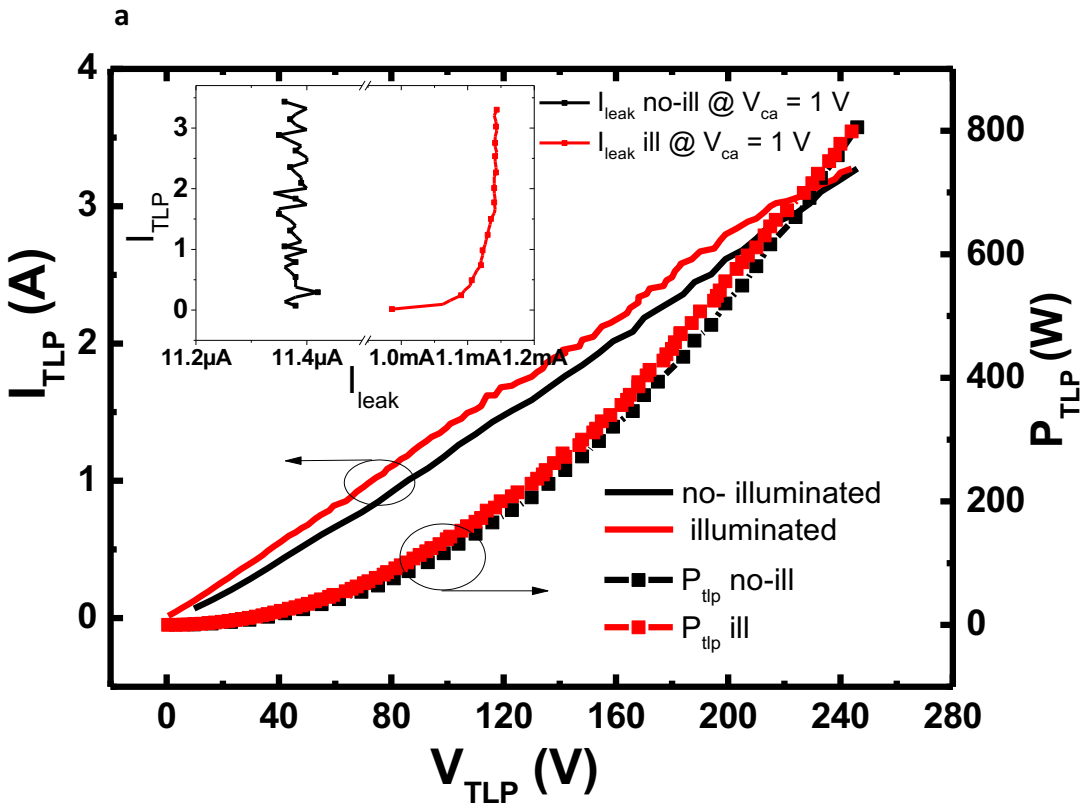
I observed that regardless of the presence of the illumination, devices tested according to i and ii do not fail (Figure 3-1). In case i, the cells sustained a TLP current (I_{TLP}) of 3.35 ± 0.12 A corresponding to an applied TLP voltage (V_{TLP}), directly applied across the pixel, of 229 ± 24 V. Similarly, in case ii, cells sustained a maximum I_{TLP} current of 3.31 ± 0.05 A corresponding to a V_{TLP} across the pixel of 251 ± 10 V. The P_{TLPMax} (see 1.3.1) measured reach a value of 767 ± 110 W and a value of 830 ± 44 W, corresponding to an E_{TLPMax} of ~ 83 μJ and of ~76 μJ (pulse mean duration 98 ns), for the case i and ii respectively. The pulsed resistance is very similar for pulse modules bigger than 50 V and it ranges

from 75.2 Ω to 92.44 Ω in case i and from 72.5 Ω to 74.2 Ω in case ii. However, the same curves are different for applied pulses lower than 50 V, resulting much higher in the case i, probably due to a different arrangement of the chains in the active layer. These values were registered for a pre-charge voltage value of 2000 V, which is the maximum voltage allowed by the instrument we used, which suggests that possibly a higher level of stress is sustainable by these devices. As shown in Figure 3-1a, there is a linear correlation between the I_{TLP} and the V_{TLP}. From the inset of the same (Figure 3-1a) we can observe the registered leaking currents measured for an applied voltage of 1 V. The one under illumination produces a higher value of current, roughly 1.1 mA, which is coherent with the normal functioning of the cell for an applied V_{AC} of 1 V. In both cases there are no signs of damages coherently with the TLP graphs. The robustness to the TLP stress shown in both the positive TLP cases arises from the fact that charges are favoured to move into the active layer from the anode (ITO-PEDOT) towards the cathode (Ca-Al) since the devices are working as diodes in forward condition, i.e. in the first quadrant, and thus devices successfully discharge the pulsed power without resulting destroyed for Joule effect[14].

In the case of negative TLP treatments (iii & iv) (Figure 3-1b) there is a clear change into the leakage current indicating that a failure is occurring. This change occurs for an I_{TR} of almost 0.2 ±0.065 A, corresponding to trigger voltage V_{TR} of 46 ± 17 V, in the case iii and for an I_{TR} of 0.49 ± 0.13 A, corresponding to a V_{TR} of 42.4 ± 7 V, in the case iv. We observe a P_{TR} of 9.2 ±6 W (E_{TR} of ~ 0.9 μJ) for the not illuminated devices and of 20.7 ± 9 W (E_{TR} of ~2 μJ) in the case of the illuminated ones. Interestingly, the slope of the graph of the devices tested under illumination is different from the one not illuminated, pointing out a different behaviour of the pulsed resistance R_{TLP} across the device during the TLP test in the two cases: ranging from 200 Ω to 214 Ω before the failure and steeply decreasing to 151 Ω after (iii); ranging from 92.7 Ω to 102 Ω before the failure and falling to 77 Ω after (iv) (Figure 3-2). The different behaviour of these devices pointed out in the negative TLP test can be explained analysing the position of the charges in the device in correspondence of the iii and iv cases. In both these cases there are a lot of p charges into the active layer, which are not favoured to move from the cathode towards the anode due to the applied field, hence all the pulsed power is discharged uniquely via a joule effect up to the point in which an irreversible damage occurs. Nevertheless, a difference was noticed between these two cases. In the case of negative applied pulses under illumination, at the moment of the pulse striking the device a negative photogenerated current is already flowing through the same so explaining the different R_{TLP} between iii and iv. The TLP pulses force the device into a reverse bias that is not favouring both

electrons and holes to move through the active layer therefore leading to the device failure anyway. I also repeated all the tests by changing the TLP step, namely 5-10-50 V, and I observed that the TLP measures are not affected by such parameter variation.

The observed R_{TLP} values, ranging between 214 Ω and 77 Ω, let OPVs possibly qualify as ESD protections in applications that feature a considerable higher input impedance of this one. Therefore, by inserting these devices in parallel to such other devices, ESD phenomena would primarily affect OPVs and, depending on the polarity of the applied pulses, the latter could also act as ESD monitor since, if applied pulses are positive the OPVs expectably continue to work, whilst result compromised if pulses polarity is negative. Instead, in case protections for OPVs need to be designed, these must avoid the pulsed energy to overcome a value of 0.32 µJ and I_{TLP} and V_{TLP} to overcome 0.13 A and 29 W respectively.



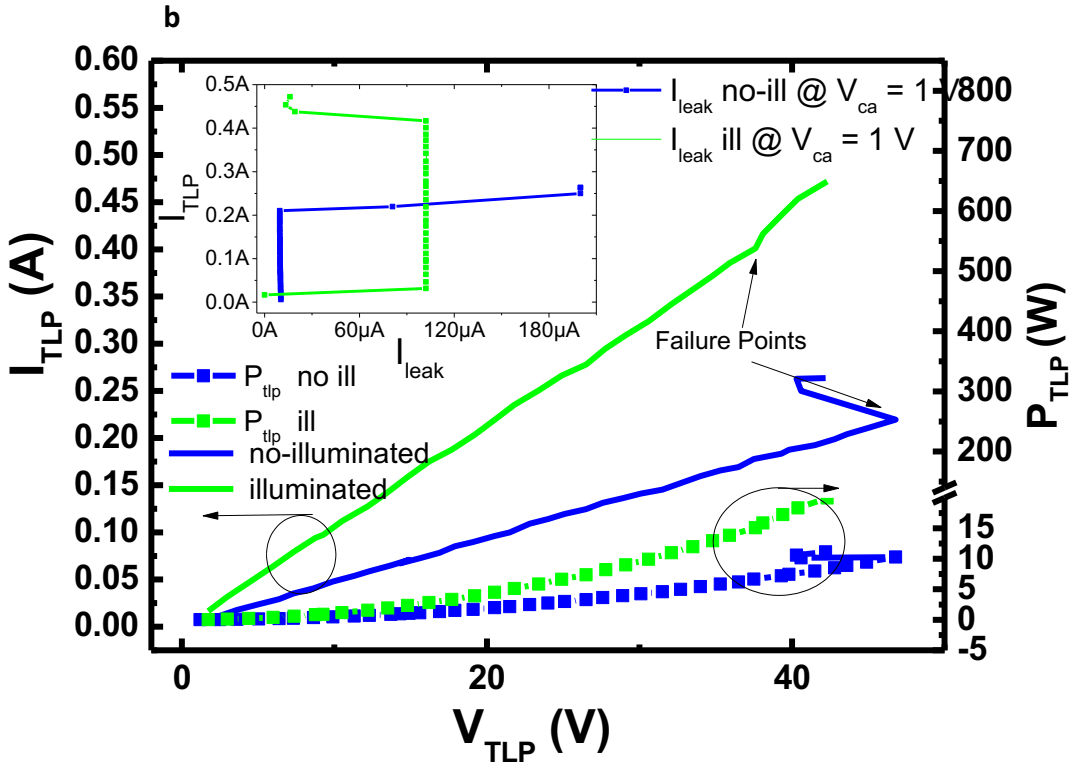


Figure 3-1: The TLP curves measured according to the positive applied pulses (a) and negative applied pulses (b). In both graphs the curves measured under illumination and in dark conditions are reported.

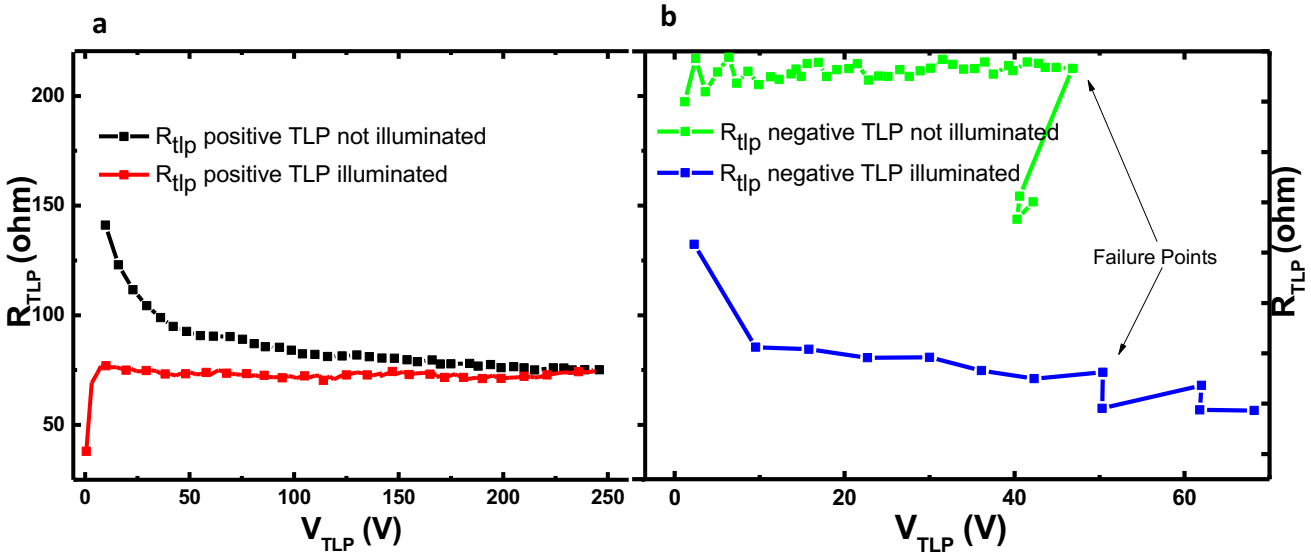


Figure 3-2: R_{TLP} of samples stressed with positive (a) and negative (b) pulses.

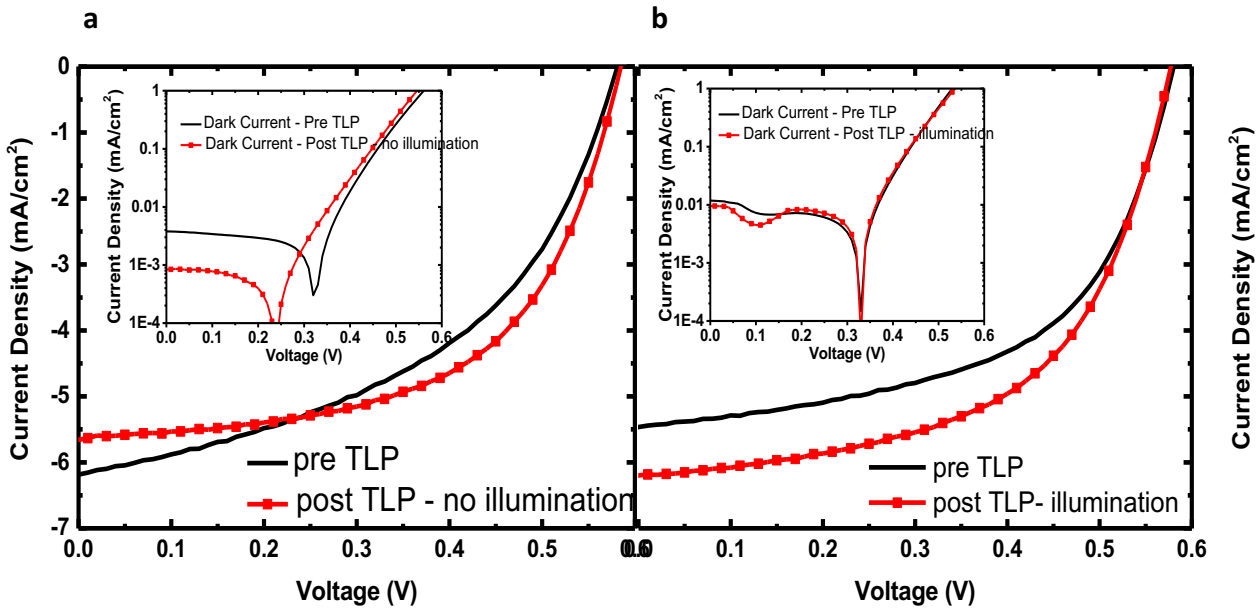


Figure 3-3: The JV curves of the cells before and after the positive TLP stress. On the right (a) the cells that were in dark conditions during the TLP and on the left (b) those kept under illumination during the TLP test. In the insets, the JV curves of the cells in dark conditions.

3.1.2 OPV Parameters

The short circuit current density (J_{sc}), the open circuit voltage (V_{oc}), the fill factor (FF) and the power conversion efficiency (η) of pristine (devices not TLP stressed) and TLP-treated solar cells in Table 1 are reported. Notably, the pristine ones features are consistent with previous paper published in our group[68]. As pointed out by the graphs in Figure 3-3, the current density vs voltage (JV) curves confirm that the OPVs maintain their functionality whenever the applied pulses between the anode and the cathode are positive. However, there are some significant differences arising after the TLP tests depending on the presence of the illumination (Figure 3.3). Firstly, J_{sc} results lowered in amplitude by ~ 7 % in dark conditions, instead in the case of illuminated devices the J_{sc} increases in modulus by ~ 13 %. The V_{oc} remains almost the same after the stress regardless of the illumination, featuring a variation contained within the ± 1 % in all cases. The average FF increases by ~ 24 % in the case of not illuminated and by ~ 0.83 % in the case of the illuminated devices. The average η improves in both cases; precisely by the ~ 13 % and the ~ 14 % respectively for not illuminated and illuminated devices. Interestingly, the TLP stress exerts a beneficial effect slightly improving the solar cells JV parameters. This effect can be seen as a consequence of the pulsed electro-annealing that stimulates a filling-effect of the charge-carrier traps present into the device due to the ions sweeping towards the electrodes. Such ions also affect the potential barrier directly interacting with

the built-in voltage. Furthermore, the polar molecules and polymer chains into the active layer are aligned according to the applied pulsed field. These phenomena altogether cause an improved yield of the devices[157], [158].

The equivalent circuit model for a solar cell[79], [80] (Figure 1-12) consists of a current generator I_L that takes in account the photo-generated current flowing through the device, of a current I_D produced by a diode that takes in account the recombination of the charges, a shunt-resistance R_{SH} parallel to the diode, taking in account the resistance across the active layer, and a resistance R_S that takes in account the loss due to the contacts. The equations describing such circuit are introduced in section 1.2.1. The general improvement of the cell can be explained as a consequence of the decrease of the R_S of the cells, possibly due to the ions migrations induced by the applied pulsed field previously described. The reduction of the charge-carriers traps also reduces the diode current that represents the exciton recombination current. R_S decrease correlates with the increase of the FF, whereas the V_{oc} negligible variation suggests that R_{SH} is not particularly affected by the treatment. The combinations of all these factors lead to the increase of the η as observed. The dark currents in illuminated devices are slightly reduced after the TLP stress, whereas significantly so in dark condition, corroborating the observed improvement of the cell. In terms of the equivalent circuit, in dark conditions the I_L is null and the measured I is directly correlated to the diode current that results hence lowered as R_S decreases, confirming the observed post-positive-TLP induced improvement.

Table 1: TLP and JV parameters after the TLP tests.

	Positive TLP not illuminated	Positive TLP illuminated	Negative TLP illuminated	Negative TLP not illuminated
TLP test	Not failed	Not failed	Failed	Failed
P_{TLPMax}	767 ± 110 W	830±44 W	9.2±6 W	20.7±9 W
I_{TLPMax}	3.35 ± 0.12 A	3.31±0.05 A	0.2±0.07 A	0.49±0.13 A
V_{TLPMax}	229 ± 24 V	251±10 V	46±17 V	42±7 V
J_{sc} pre TLP	6.4±0.1 mA/cm^2	5.3±0.2 mA/cm^2	5.6±0.5 ma/cm^2	5.8±1.7 ma/cm^2
J_{sc} post TLP	5.9±0.4 mA/cm^2	6±0.2 mA/cm^2	Not working	Not working
Δ J_{sc}	-7.2±3.5%	+13.1±0.7 %	-	-
V_{oc} pre TLP	0.587±0.002 V	0.575±0.005 V	0.565±0.036 V	0.578±0.009 V
V_{oc} post TLP	0.585±0.569 V	0.576±0.001 V	Not working	Not working
ΔV_{oc}	-0.34±0.4 %	+0.17±0.9 %	-	-
FF pre TLP	46.8±0.4 %	53.1± 2.2 %	53.3±0.1 %	49.3±0.3 %
FF post TLP	58.1±1.7 %	53.5±2.3 %	Not working	Not working
ΔFF	+24.3±4.7 %	+0.8±1.1%	-	-
η pre TLP	1.79±0.03 %,	1.62±0.14 %,	1.97±0.16 %	1.6±0.41%
η after TLP	2.01±0.18 %	1.85±0.16 %	Not working	Not working
Δη	+13.15±8.2 %	+14.2±1.3 %	-	-

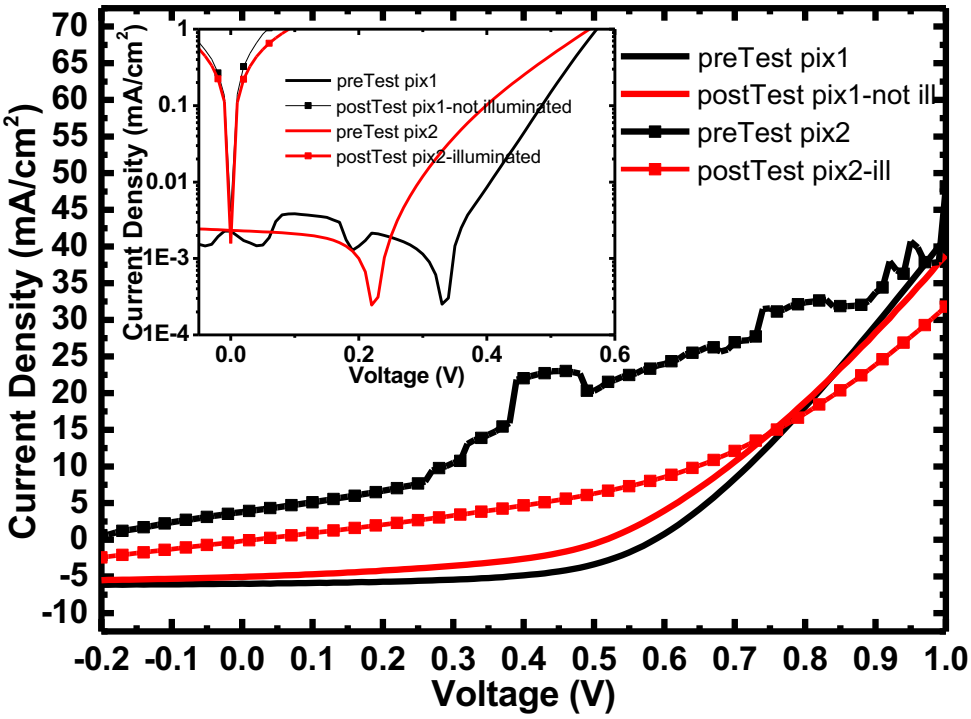


Figure 3-4: the JV curves of the cells before and after the negative applied pulses, for both the cases in which the devices were illuminated and not.

In the case of negative applied pulses, the reverse pulsed bias applied causes the breakdown of the junction (Figure 3-4). In fact, as long as the device provides to the striking pulse a way to be dissipated, or rather a way to be discharged, this can withstand the applied power. On the opposite, when the junction is in reverse the current is not normally allowed to flow through it, and thus the incoming power starts being dissipated mainly via Joule effects that progressively spoils the device. In all cases analysed, in correspondence of the I_{TR}, the linear dependence between V_{TLP} and I_{TLP} ends revealing the point in which a permanent damage into the device occurs. Notably, also in the I_{LEAK} vs I_{TLP} graphs there is a sudden increase of the I_{LEAK} in correspondence of the I_{TR} value, (Figure 3-1.b inset) pointing out the arising of a current flowing into the junction due to the breakdown thereof. Referring to the equivalent circuit (Figure 1-12) the breakdown is the result of a sudden dramatic decrease of the R_{SH} that discharges the current I_L. Although the response to negative applied pulses results in a permanent damage of the devices in both the illuminated and not illuminated devices, there are few differences that are worth discussing. In the case in which no light was applied, I observed a lower value of power tolerated by the device in comparison of the one of the case in which they were illuminated, as also confirmed by Figure 3-1.b. In the case of the illuminated devices, the striking current is partially dissipated via the negative photo-generated current due to

the impinging light. In the case of not illuminated devices the incoming power cannot be discharged but via Joule effects so generating a lower value of P_{TR}. When devices are not illuminated the power dissipated into the active layer can dig a hole into this, thus leading to a short circuit[159], which I observed in two of the three devices tested in dark conditions. Any such treated device reveals a response to the pulsed field similar to the one of a dielectric kept between two electrodes. On the contrary, the illuminated devices feature the behaviour observed in a junction brought to the breakdown but not turned into a short circuit[160].

3.1.3 **PL spectra**

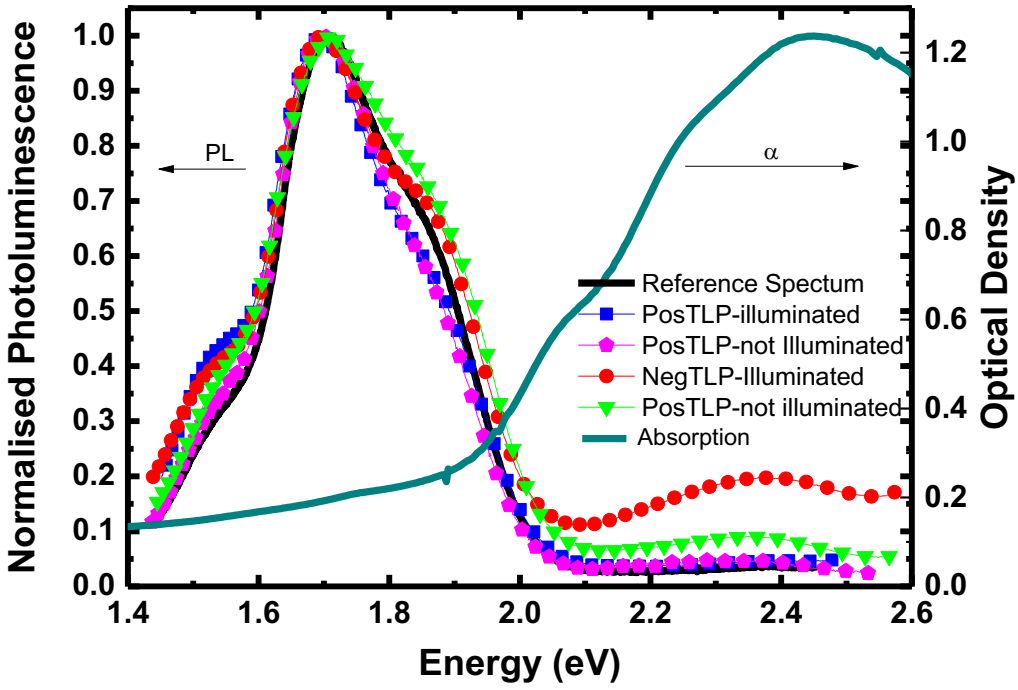


Figure 3-5: Normalised photoluminescence and absorption spectra of TLP stressed devices.

From the PL spectra (Figure 3-5), obtained by exciting the films with a 450 nm (2.75 eV) diode laser, there are four notable peaks in the complex P3HT-PCBM: namely a first peak at 1.52 eV reasonably due to the vibronic 0-2 emission peak of the P3HT (i)[68], [161]–[163]; a second one at 1.69 eV where interestingly both the PCBM single excited emission and the vibronic 0-1 emission peak of the P3HT take place (ii)[163]; a third one at 1.85 eV reasonably due to the vibronic 0-0 emission peak of the P3HT (iii); a fourth at 2.37 eV due to a charge-transfer (CT) transition of intermolecular

exciton (iv)[45]. I used as reference the PL obtained from the pixels of a not stressed device, which showed a similar response in all pixels tested. Interestingly, in peak iii the relative ratios between the vibronic 0-0 peaks in TLP stressed devices and the same peak from the reference results lower than 1 in positive TLP-stressed devices whilst higher than 1 in negative TLP-stressed ones. Analogously, the peaks in iv also change according to the polarity of the TLP tested used, resulting very low or nearly absent in the reference and the two positive stressed cases spectra, instead increasing significantly in the peaks of the negative treated devices, especially in those that were kept in dark conditions during the negative TLP test. These PL spectra therefore show a correlation between the polarity of the TLP test and the peaks relative intensity. The positive TLP test performs an electro-annealing of the devices that induces a further mixing of the two components in the active layer, therefore improving the photovoltaics parameters. The reduction of the vibronic 0-0 peak of the P3HT and the confirmed absence of the CT transition peak of the PCBM corroborate such explanation. On the contrary, the negative pulses trigger an isolation of the two components, either by damaging P3HT chains and PCBM molecular structures or by randomly promoting crystal domains formation, which weakens the exciton splitting mechanism and increases the PL emissions of the two separate species. In particular, the CT transition peak at 2.4 eV that is normally quenched for PCBM molecules mixed with P3HT or other donors, clearly indicates that a certain number of PCBM molecules are no longer able to interact with the P3HT chains after the negative TLP test. The separation of the two species into the active layer is coherent with the loss of the photovoltaics features of the devices.

3.1.4 Effect of V_{oc} bias on samples robustness to TLP stress

I also repeated the TLP test by applying pulses on devices biased with a V_{AC} voltage equal to the measured V_{oc} of the cells for illumination conditions. I did not perform such test in dark conditions since the balancing of the external field with the built in one requires the cell to be under illumination conditions. Such condition is not normally exploited in solar cells but, nevertheless, is an important condition that reveals if the built-in voltage of devices is the one expected in regard to the materials used to build the active layer of the cell. In fact, the calculated V_{oc} is equal to 0.6 eV (equation 1.2) for P3HT:PCBM heterojunction solar cells but commonly the value measured is around 0.56 eV. The discrepancy arises due to factors such as contaminations, oxidation and degradation of materials during the fabrication process. Hence, the displacement of the measured V_{oc} value from the calculated one is a measure of the quality of the cell.

The TLP test carried on in these conditions damaged 2 out of 3 tested devices during the positive TLP test as well as during the negative TLP. This reveals a weakening of the cells in such conditions, in comparison with positive pulses applied to the cell in correspondence of no applied V_{AC} bias and under illumination. Importantly, a similar behaviour arises regardless of the pulse polarity, reasonably due to the fact that no charges are supposed to flow in such conditions, since a balance is reached if an external applied field nulls the built in one. Hence, upon an applied pulse, either positive or negative, the supplied energy is dissipated via a Joule effect that in most of the cases causes a breakdown of the active layer, with the cell assuming a resistor-like linear behaviour. The I_{TLP} was found between 3.78 A and 2.48 A in those tested with positive pulses and between 3.52 A and 1.93 A in those tested with negative pulses, respectively corresponding to a V_{TLP} ranging from 199 V and 464 V and from 146 V and 461 V. The behaviour of the R_{TLP} is shown in Figure 3-6, beside the first pulses the curve shape is similar in both cases, revealing a slightly higher value of resistance in correspondence of the negative pulses, namely of 10 Ω roughly, probably due to the P3HT charge carrier mobility resulting slower in the second case. In fact, the R_{TLP} ranges between 37.85 Ω and 16.61 Ω in those stressed with positive pulses and between 51.52 Ω and 39 Ω in the others. From the I_{TLP} vs V_{TLP} graphs it is not possible to observe a clear failure (Figure 3-6), nevertheless the JV curves of devices compared before and after the test reveal that a permanent damage of solar cells occurred (Figure 3-7) and a linear behaviour can be observed.

The V_{oc} bias moved the charges in such a way that weakened the overall robustness to electrostatic discharges confirming that the position of the charges into the active layer is crucial for the dissipation of the striking pulse, as long as the metal connections are big enough to withstand the current flowing through them.

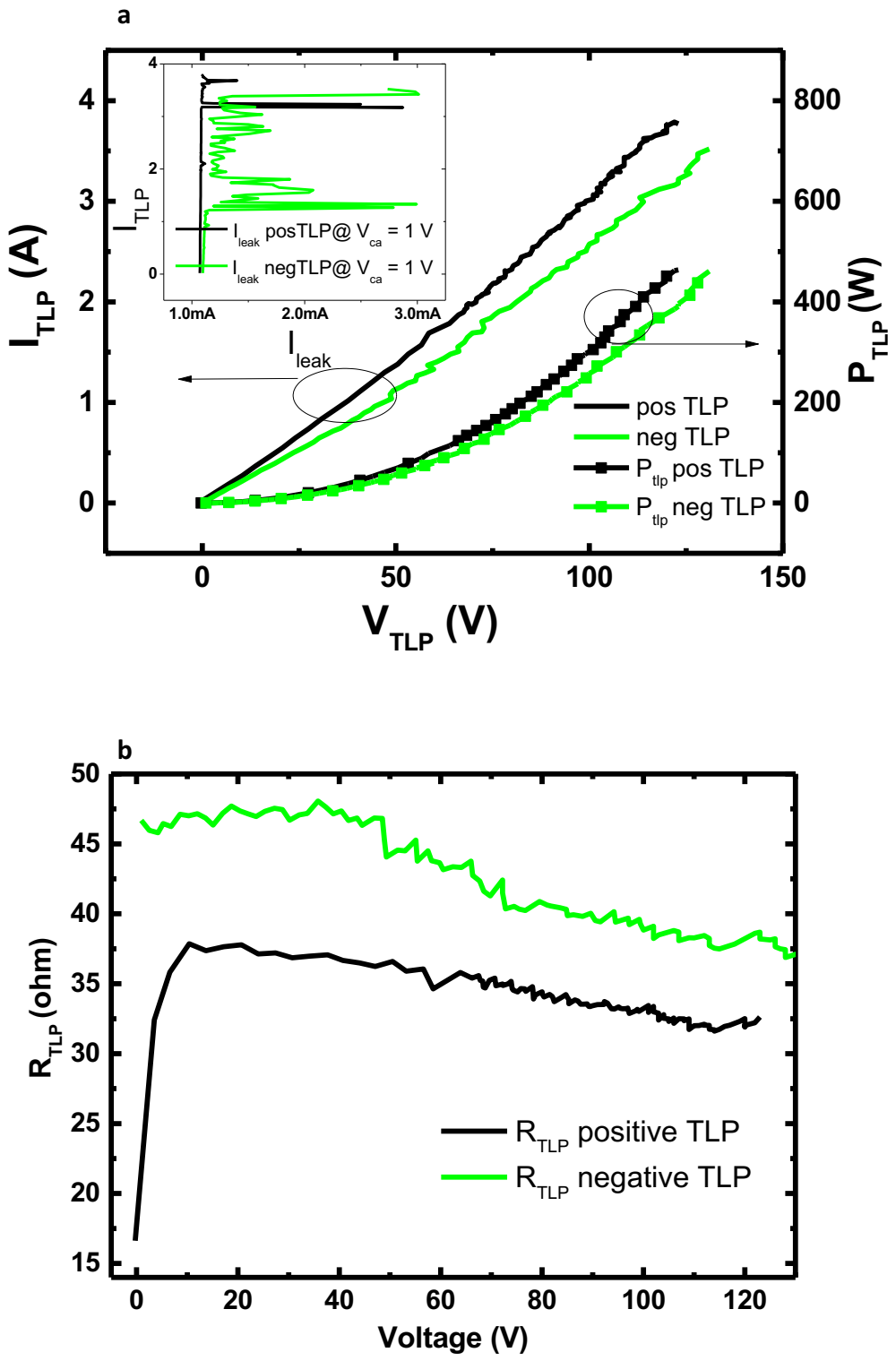


Figure 3-6. The TLP graphs of V_{oc}-biased solar cells (a) in which the behaviour is similar regardless of the pulse polarity. (b) The graph of the behaviour of the R_{TLP} in both positive and negative TLP cases is reported.

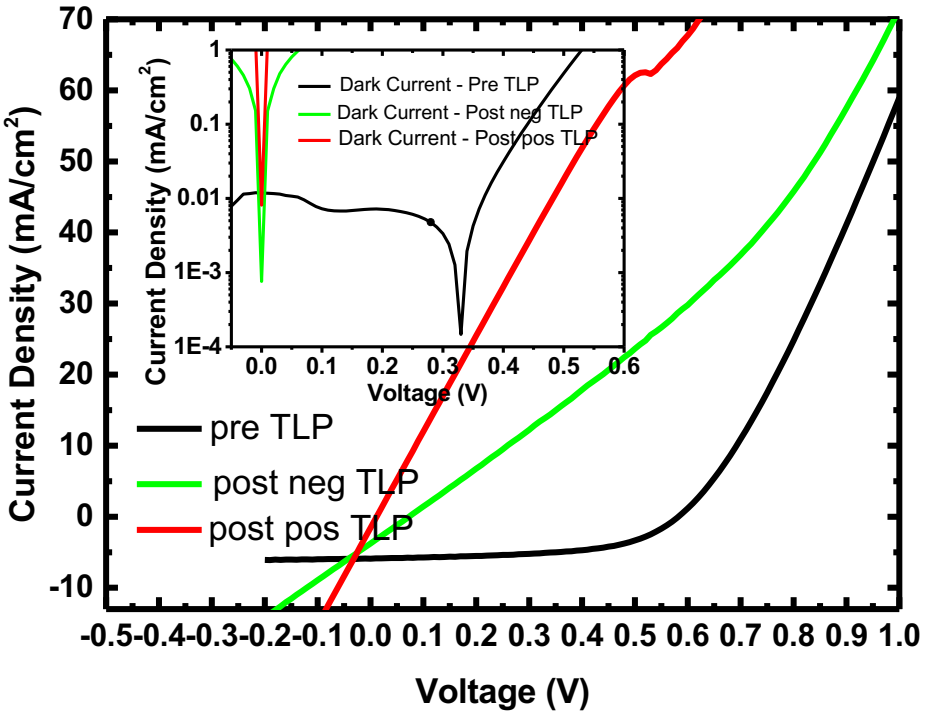


Figure 3-7: the JV graphs of pixels tested before and after the TLP test carried out in correspondence of an applied V_{AC} bias equal to V_{oc} .and for both pulse polarities.

3.1.5 Conclusions

I investigated the response to a TLP test of P3HT:PCBM solar cells mimicking all the possible environmental scenarios these devices can undergo in case are hit by electrostatic discharges. I used negative and positive pulses applied when the cells were not illuminated and illuminated. Interestingly, in all cases analysed in which positive pulses were applied, the cells tested withstand currents higher than 3 A and dissipate an incoming power higher than 800 W without incurring permanent damages. Furthermore, I also noticed that the photovoltaic parameters of such devices result improved with a final η increased of roughly 14% respect to the pristine ones. On the other hand, the same devices resulted much weaker in the case of negative applied pulses, which means that protections are required and must be designed considering the minimum I_{TR} found to be 0.13 A. Focusing more on the devices and describing the JV parameters changes in OPV equivalent electronic circuit terms, the positive pulses exert an electro-annealing of the devices that reduces the R_S that in turn causes an improvement of the FF and consequently of the η. The R_S reduction can be explained as a consequence of the ions into the device forced by the pulsed applied field to

migrate towards the electrodes and in remaining trapped into the charge-carrier traps. The V_{oc} is not affected by the positive pulses, hence the R_{SH} does not vary during the test. The cells behaviour in dark conditions feature a reduction of the dark current therefore corroborating the general improvement observed. However, the negative pulses dramatically reduce the R_{SH} causing a reduction of the V_{oc} and a loss of the functionality of the devices. Interestingly, PL spectra highlighted a correlation between the failure of the devices and the split of the two phases composing the active layer. Upon positive pulses, the two phases result further mixed so leading towards a quench of the vibronic 0-0 peak and of the CT peak of the PCBM, whilst the same peaks are enhanced in the negative TLP tests, possibly due to a relative reciprocal isolation of the two species that no longer permits an energy exchange between the P3HT chains and PCBM molecules.

Interestingly, OPVs can act as ESD protection and pulse polarity monitors if placed in parallel to other devices having an input impedance higher than the R_{TLP} observed in OPVs, which considering all cases analysed spans between 10 Ω and 214 Ω. In fact, upon applied negative pulses OPVs would result in a failure, whilst they expectably keep on working upon applied positive pulses. On the contrary, if OPVs need to be ESD shielded, protections must avoid incoming ESD to overcome a pulsed energy of 0.32 μJ and I_{TLP} and V_{TLP} to overcome 0.13 A and 29 V respectively.

Organic semiconductors have been captivating great attention in the last years for their cheap and easy manufacturing, their suitability for flexible devices. A further advantage respect to the inorganic counterpart is pointed out in this study, revealing the exceptional robustness they feature towards ESD positive pulses.

3.2 TLP test on P3HT and PBTTT OFETs

In this section, I report on the effects of TLP stress on the IV curves, the threshold voltage (V_{TH}), the mobility and the on/off ratio of P3HT and PBTTT OFETs.

The TLP characterisation exploits the same system also used for OPVs and OLEDs (see 2.5). In this case I carried out four different analysis modes, obtained by changing the terminals from which the TLP pulses were applied and their polarity: i) positive pulses between the drain and the gate terminals (DGpos) with source terminal left floating; ii) negative pulses between the drain and the gate terminals (DGneg) with the source terminal left floating; iii) positive and iv) negative pulses between the drain and the source terminals (DS) with the gate contact biased according different voltages. A test in which positive pulses between the source and the gate are applied (SGpos) is

equivalent to the DGpos whilst a test in which negative pulses between the source and the gate (SGneg) are applied is equivalent to the DGneg, therefore for such reasons the SGpos and the SGneg tests were not carried out. DS tests, instead, were further subdivided in other tests depending on the bias applied, by means of a third terminal, to the gate of the device under test (DUT), namely: positive applied pulses with gate grounded (DSpos); negative applied pulses with gate grounded (DSneg); positive applied pulses with a gate bias of 10 V (DSpos10$V_g$bias); negative applied pulses with a gate bias of 10 V (DSneg10$V_g$bias); positive applied pulses with a gate bias of -20 V (DSpos-20$V_g$bias); negative applied pulses with a gate bias of -20 V (DSneg-20$V_g$bias).

The I_{LEAK} is measured for an applied V_{DS} voltage of -20 V and V_{GS} =-40 V. Such TLP setups were used for both P3HT and PBTT OFETs. According this conditions the current flowing between the drain and the source of a P3HT OFET is expected to be between -5 μA (20 μm-channel length) and -50 μA (5 μm-channel length) as shown in Figure 3-8, whereas between -20 μA (20 μm-channel length) and -200 μA (5 μm-channel length) for PBTTT OFETs (Figure 3-9). Therefore, I set as failure criterion an I_{LEAK} >0.5 mA which would mean having more than a tenfold increase of the current flowing through the drain and the source in P3HT OFETs and more than the double in PBTTT OFETs, conditions consistent uniquely to a failure causing short circuits or low-impedance induced paths to current. I also measured the I_{LEAK} in a different spot, namely for V_{DS}=V_{GS}=-40 V but all the results here reported are referred to the previous one specified and no significant differences were observed between the results obtained using this second spot. The devices here studied and discussed were fabricated according the procedure highlighted in section 2.3, whereas their characterisation was obtained by using the setup described in 2.3.1. The Raman spectra collected from these devices, instead, were obtained according the methodology pointed out in 2.6.2.

In the first part of this section I report about the electric features (V_{TH}, μ, on/off) of pristine P3HT and PBTTT OFETs, where for pristine is intended characterised straight after ending their fabrication procedure. In the second part of this section the results obtained on P3HT OFETs are reported, namely: the TLP results I obtained per each of the study-case analysed; a comparison between pristine and TLP-treated device electric features whenever the functionality of the latter was maintained; the results of Raman spectroscopy analysis carried out on pristine and TLP treated devices. Whereas, in the third part those regarding PBTTT OFETs are reported and structured as done for P3HT. Each of these two parts are concluded with a discussion about the results observed. Final considerations about both P3HT and PBTTT OFETs are then reported in the last part of this section.

3.2.1 OFETs pristine electrical parameters

3.2.1.1 *P3HT-OFETs pristine samples electrical parameters*

I observed hysteresis affecting the majority of the devices, which is a phenomenon in OFETs due to multiple factors such as the trapping of the charges at the semiconductor-dielectric interface, the slow reaction of the polymer charge carriers to the applied electric field[99]. These phenomena are common to both P3HT and PBTTT. The maximum amplitude of the drain-source current (I_{DSMAX}), measured for an applied V_{DS} of -80 V and V_{GS} of -80 V in the transfer curve, is inversely proportional on the channel length (Equation 1.9 and 1.10). The 20 µm-channel length transistors feature an I_{DMAX} of -42.13±11 µA, whilst the 10 µm -131.07±35 µA and the 5 µm -508.94±150 µA. In all cases for an applied V_{GS} of 0 V the transistors are in off-state mode, with a measured I_{DS} always lower than 1 µA. In Figure 3-8 output and transfer characteristics of the 20 µm, the 10 µm and the 5 µm channel length transistor are reported. The charge carrier mobility in the saturation region of these devices is 9.6±1.5 $x10^{-3}$ cm^2/Vs, whereas the threshold voltage is -17.1±5.6 V and the on/off ratio is 0.9±1.3 $x10^4$ (I_{DS} measured for an applied V_{GS} of -80 V and V_{DS} of -80 V divided by the I_{DS} measured for an applied V_{GS} of 0 V and V_{DS} of -80 V). The electrical characteristics of these P3HT-transistors are consistent with previous literature[92], in particular Seidler et al.[68] observed a charge carrier mobility of ~$10x10^{-3}$ cm^2/Vs for P3HT OFETs.

3.2.1.2 *PBTTT-OFETs pristine electrical parameters*

Pristine PBTTT OFETs were showing an on/off ratio of $0.6x10^4$ (measured for an applied V_{DS} of -80 V and by dividing the I_{DS} measured in correspondence of the V_{GS} equal to -80 V and to 0 V) whereas the mobility was found equal to 6.9±2.7 $x10^{-2}$ cm^2/Vs. The V_{TH} was found equal to -9.25±2.4 V. As regards the I_{DSMAX} registered for an applied V_{DS} of -80 V and V_{GS} of -80 V, its value was found equal to -0.88±0.13 mA, -2.28±0.46 mA and -8.92±1 mA respectively in 20 µm, 10 µm and 5 µm channel length transistors. In all cases for an applied V_{GS} of 0 V the transistors are in off-state mode, with a measured subthreshold current I_{DS} lower than 40 µA. These value are consistent with features reported in literature[96] and were calculated per each channel length considering 12 devices spread over three different substrates. In Figure 3-9 the transfer and output characteristics of the 20 µm, of the 10 µm and of the 5 µm channel length PBTTT OFET prior the TLP treatment are reported.

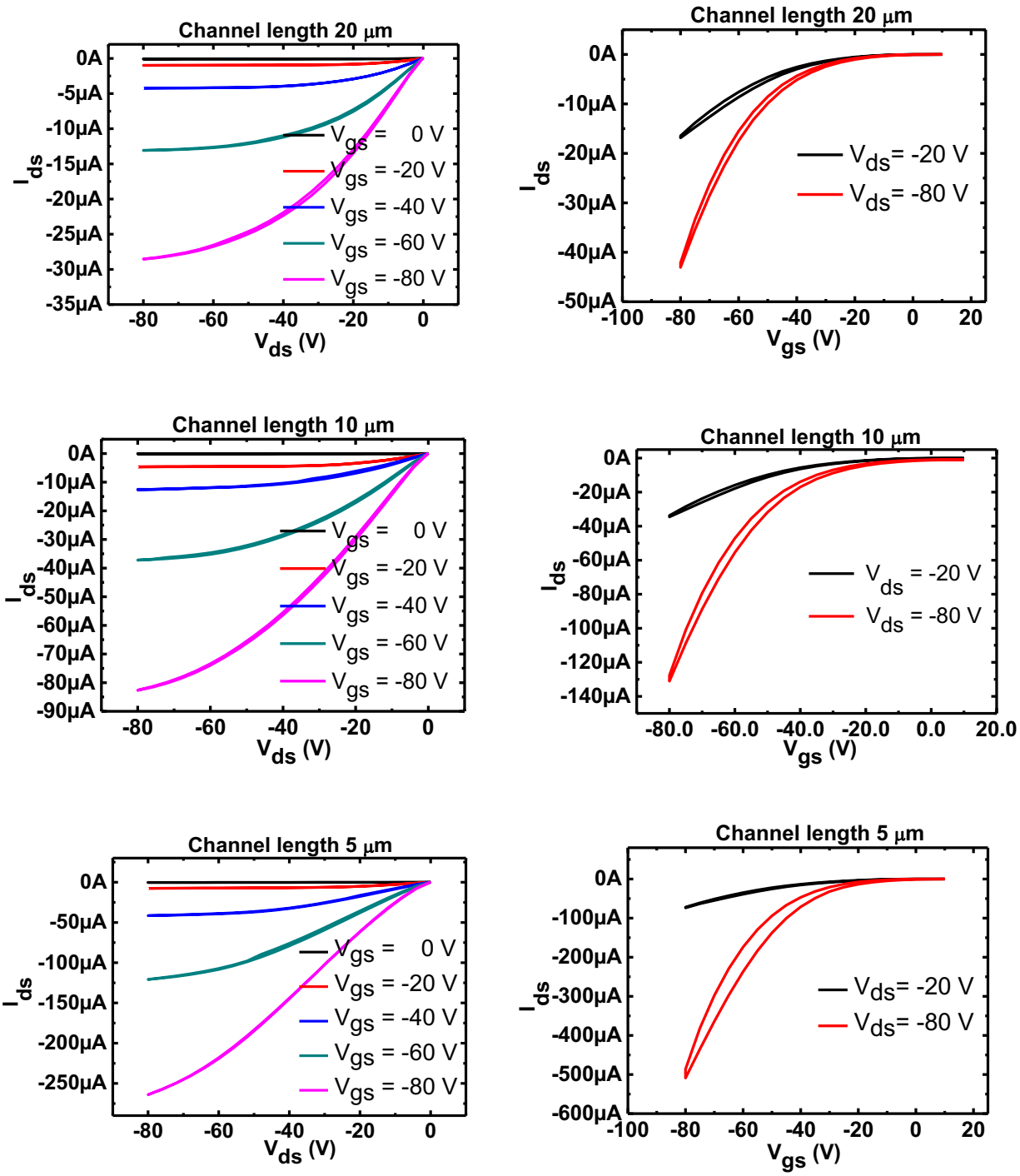


Figure 3-8: The Output characteristics and the transfer characteristics of the 20 µm, of the 10 µm and of the 5 µm channel length P3HT OFETs.

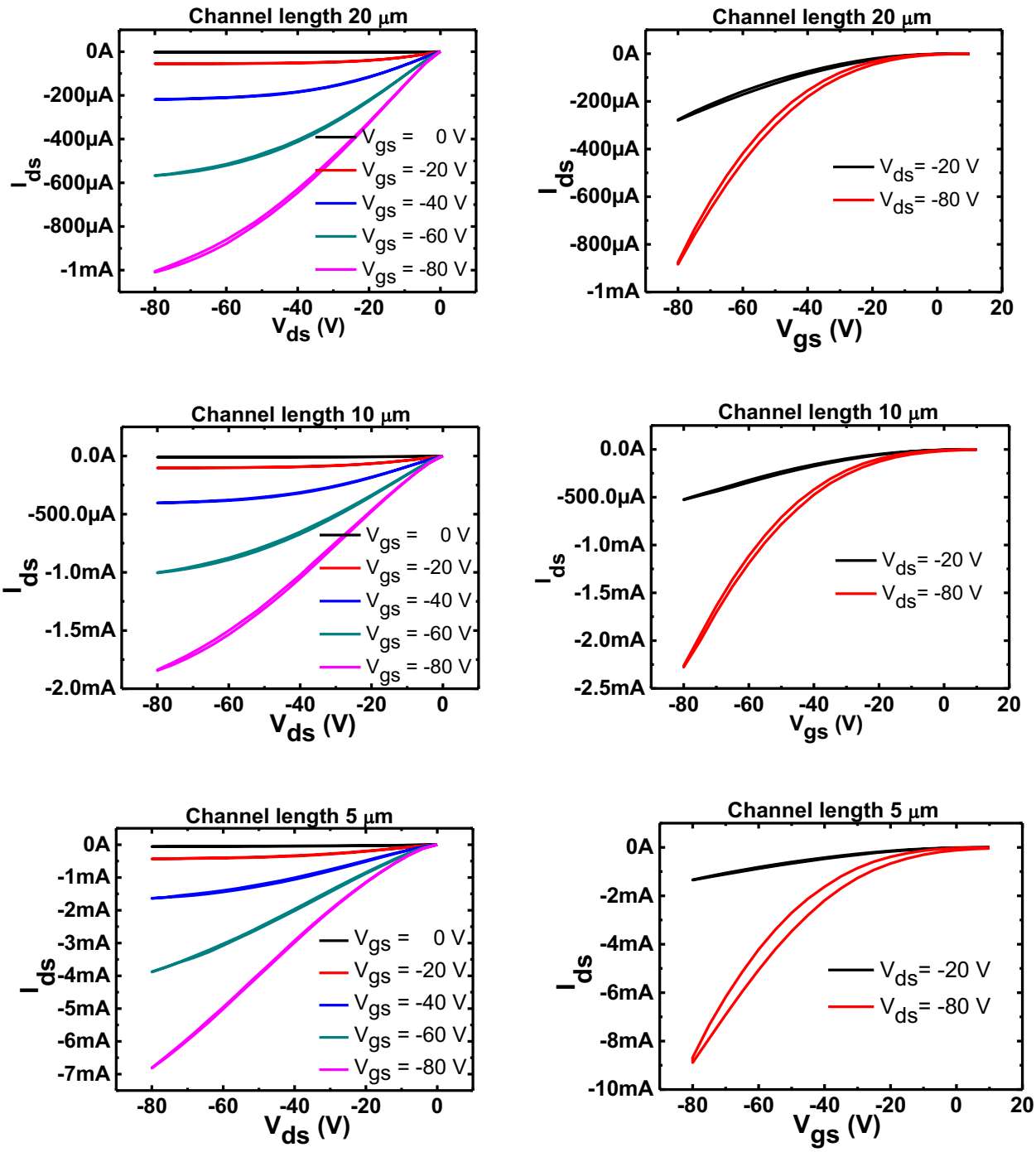


Figure 3-9. The Output characteristics and the transfer characteristics of the 20 μm, of the 10 μm and of the 5 μm channel length PBTTT OFETs.

3.2.2 TLP results on P3HT OFETs

I prepared P3HT OFETs to characterise the response to ESD phenomena of such devices. In this section, I report on the results obtained for the TLP treated P3HT OFETs.

3.2.2.1 *P3HT Positive Drain-Gate TLP-test (DGpos)*

The DGpos tests were carried out on all the transistors of the chip. After each applied pulse, the status of the transistors was evaluated by measuring the I_{LEAK} for an applied V_{DS} of -8 V and an applied V_{GS} of -40 V. The value of V_{DS} and of V_{GS} were chosen according to reported works in which P3HT transistors were applied in electronic circuits[94], [164]. As failure criterion, I arbitrarily chose the increase of the I_{LEAK} over 1 μA since, in normal conditions, the current flowing between the gate and the drain is as low as 10^{-12} for the OFETs in this thesis analysed. I observed the failure of the device in all the cases analysed. The destruction of these devices stems from the breakdown of the silicon oxide, thus resulting in a dramatic increase of the current flowing between the drain and the gate. All devices show a break-point around an applied voltage across the terminals (V_{TR}) of 315 V and a current flowing through the terminals (I_{TR}) of 0.09 A (Figure 3-10a, representative for all cases), regardless of the channel length of the transistor tested. The failure appears to be progressive, since both I_{TLP} and the I_{LEAK} increase according to the module of the applied voltage, with the latter reaching the compliance current (1 μA). The dielectric breakdown of the silicon oxide that I observed is approximately 13.6 MV/cm (obtained considering the thickness of the gate, 230 μm, and the voltage across the same causing the breakdown, 315 V), slightly higher than values reported in literature for silicon oxide, where a breakdown is normally observed between 2 MV/cm and 10 MV/cm[165]. I used different voltage-steps for the applied V_{TLP} (10 V, 20 V and 50 V) but I observed the same response in all cases analysed therefore indicating that cumulative stress effects do not influence the dielectric breakdown of these devices.

The failure of the devices is confirmed by a direct current (DC) test in which the I_{DS} has been measured prior and after the TLP applying a V_{GS} of -40 V and sweeping the V_{DS} between -10 V and +10 V (Figure 3-10b). After the test I_{DS} overcomes the compliance current (1 mA), confirming the presence of a permanent damage[115], [116]. The current is now flowing directly through the silicon oxide, expectably broken in correspondence of the area immediately below the drain contact, therefore short-circuiting the drain with the n doped gate contact. In fact, the source was not involved during the tests.

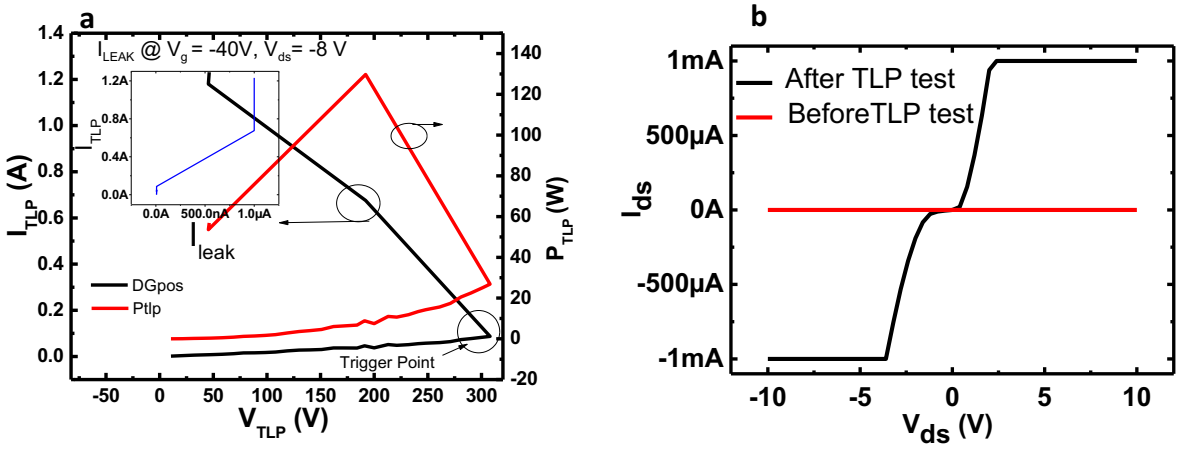


Figure 3-10: The results of a DGpos TLP test on a 10-µm channel length transistor (a). The failure occurs for an applied voltage across the terminals of 315 V, corresponding to a current flowing through these of 0.09 A. The I_{DS} measured in a 10-µm channel length transistor before and after the TLP test for an applied V_{GS} of -40 V and a V_{DS} sweeping between -10 V and +10 V (b). The I_{DS} current reaches the compliance current after the TLP, confirming the damage of the silicon oxide.

3.2.2.2 *P3HT Negative drain-gate TLP test (DGneg)*

The DGneg tests were carried out on all of the transistors of a chip. I used the same failure criterion used for the DGpos tests, measuring the I_{LEAK} in the same conditions. It is interesting to note that this time none of the transistors showed a clear failure during the TLP tests since the current flowing through the terminals was always lower than 30 nA, even though the I_{TLP} showed a sudden increase at 0.2 A corresponding to a V_{TLP} of approximately 168 V. The final I_{TLP} was of almost 4 A in all the analysed cases (Figure 3-11a). The DC test, measured in the same conditions mentioned in the DGpos test, did not show a clear change in the I_{DS} (Figure 3-11b). Hence, I measured the IV curves of such transistors and from a comparison between the ones prior to the TLP test I observed a clear degradation of the devices. In Figure 3-12 the output and the transfer characteristics prior and after the TLP test of the same transistor, a 10 µm channel length one, are reported. The silicon used in the bottom contact of the substrates is an n-doped one; upon a negative stimulation from the TLP terminals the charges moving against the silicon are the positive ones, namely holes, but these are too few to cause a complete break of the oxide therefore resulting in a dramatic increase of the current through the silicon oxide. Nevertheless, a permanent damage occurs anyway. In the case of the DGpos, the charges moving against the oxide are electrons, abundant enough to break the silicon oxide completely. Similarly to the DGpos test, the channel length does not affect the response of devices. In both DGpos and DGneg tests, the charges of the P3HT are not directly

involved in the damaging of the silicon oxide since their reactivity is by far lower than the ones of the n-doped silicon of the contacts.

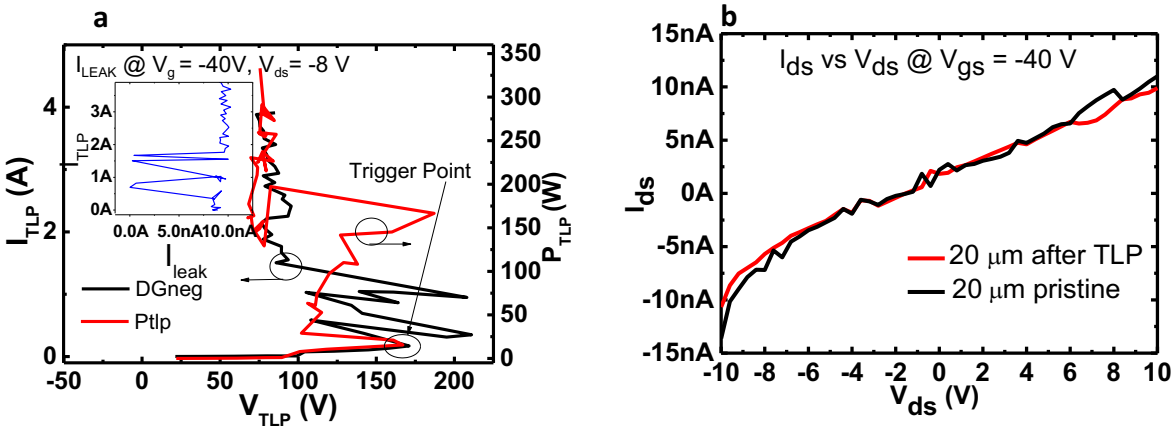


Figure 3-11: The TLP results of a 10-µm channel length transistor carried out in DGneg mode (a). The post TLP DC test of a 20-µm (b), the behaviour of the I_{DS} seemingly does not change after the TLP test. Representative for all cases.

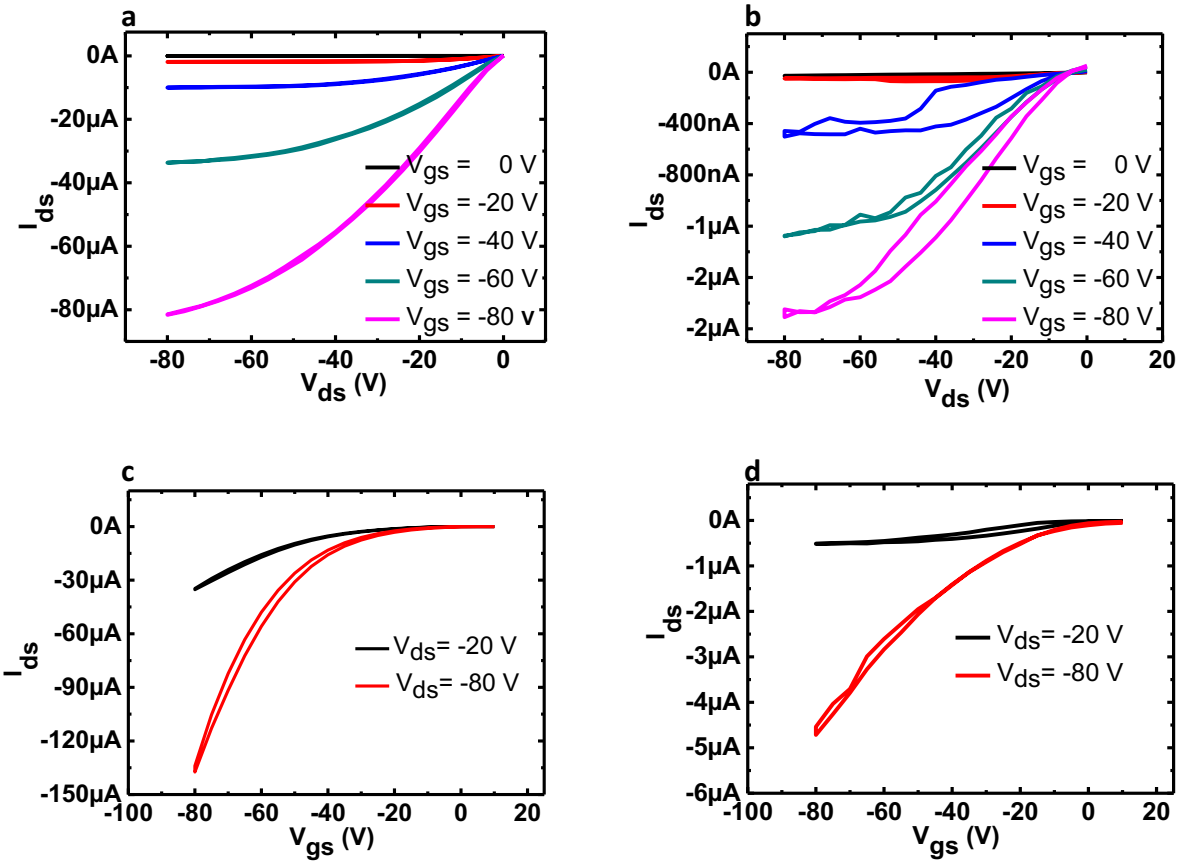


Figure 3-12: The output characteristics of a 10-µm channel length transistor before (a) and after (b) the TLP test and the transfer characteristics of the same transistor before (c) and after (d) the TLP test.

3.2.2.3 *P3HT Drain-Source TLP test*

In the following sections the DSpos, DSneg, DSpos10$V_g$bias, DSneg10$V_g$bias, DSpos-20$V_g$bias and DSneg-20$V_g$bias tests are respectively reported. Each section is so structured: a summary-table of all parameters extracted from TLP tests ($I_{TR,}$ V_{TR}, P_{TR}, E_{TR}, R_{TLP}); a summary-table of the electrical OFETs parameters (on/off ratio, mobility, V_{TH}) prior and, where possible according to the caused degree of device degradation, subsequent the TLP tests; a description of the I_{TLP} vs V_{TLP} graphs, of the I_{TLP} vs I_{LEAK}, of the DC and IV curves prior and after the exposure to the TLP stress; a top-view pictures of the TLP treated devices.

The graphs reported in each section are referred to one of the devices tested according to the TLP modality described in the section. Although such device is in turn characterised by one of the three possible channel lengths, which is a factor introducing sensible differences between the TLP parameters obtained from devices treated in the same conditions, the graphs reported are to be intended as representative of all the devices related to the section and any difference due to the channel length, or other factors, are highlighted in the text. All the tests involving the drain and the source of the transistors were carried out by choosing as TLP-failure criterion an I_{FAIL} of 0.5 mA, as explained in section 3.2. The I_{LEAK} is measured in correspondence of an applied V_{DS} of -20 V and an applied V_{GS} of -40 V[164]. The current pulse duration is set to 100 ns whilst the rising time and the descending time to 5 ns, however, the true duration can vary at each replica, and thus, the TLP system gives back a measure of the mean value of the duration of the applied pulses that must be taken in account for a correct calculation of the E_{TLP}. The pulse amplitude increasing-step was set to 10 V. Each test was conventionally decided to be stopped within 5 pulses after the arising of a snapback, hence the number of pulses applied, and consequently of the maximum pre-charge voltage used, is depending on each device response. Before and after each TLP test, a DC test was performed to evaluate the functionality of devices. The DC test is performed by applying a V_{DS} voltage sweeping between 0 V and -40 V and a V_{GS} voltage kept at -40 V throughout the DC test. None of the device contacts were left floating during the tests. The statistics obtained regarding the TLP parameters are obtained out of 4 devices with the same channel length and tested in the same TLP conditions. In regard to the electrical parameters of the OFETs (mobility, on/off ratio, I_{DSMAX}, V_{TH}), where possible depending on the resulting degree of damaging after the TLP stress, a comparison of each device features with its own pristine ones in terms of percentage variations is reported.

In section 3.2.2.4 a Raman spectroscopy investigation of all P3HT TLP-tested devices is reported, whereas in section 3.2.2.5 a discussion of obtained results obtained about TLP tests involving the drain and the source of the P3HT OFETs and those regarding the Raman spectra is reported.

3.2.2.3.1 Positive Drain-Source-no Gate bias (DSpos)

The DSpos test irremediably damaged all the transistors tested, particularly altering the off-state of these devices and forcing them to lose a proper transistor behaviour. None of them failed the I_{LEAK} test, which resulted always lower than 200 µA, and thus lower than the I_{FAIL} value (0.5 mA). None of the devices suffered a short circuit due to the test.

In the I_{TLP} vs V_{TLP} graphs (Figure 3-13), a snapback, namely a sudden increase of the I_{TLP} for a certain critical value of applied V_{TLP} followed by a region featuring a negative differential resistance behaviour[14], was observed. Such behaviour is the first evidence of the arising of a permanent damage into the device. The critical V_{TLP} from which the snapback region starts, the trigger voltage V_{TR}, decreases according to the channel length of the transistors. The $V_{TR,}$ the I_{TR}, the P_{TR} and the E_{TR} statistical values (from now on referred as TLP parameters) obtained per each channel length are reported in Table 2. The E_{TR} was obtained considering that the mean TLP pulse duration pointed out by the TLP system is 85.65 ns. The R_{TLP} was found progressively reducing with the channel length and spanning between a maximum value of 4 kΩ (20 µm-channel length) to a minimum of 1.3 kΩ (5 µm-channel length), too high to use these OFETs as protections. The scaling of the channel length results in a higher current flowing through the drain and the source, thus for shorter channels the maximum current over which the snapback starts is reached for lower values of V_{TLP} (Figure 3-14). The $I_{LEAK,}$ instead, was found to decrease during the tests, indicating a degradation of the metal contacts and of the interdigitated pattern of the transistors, as confirmed in Figure 3-15. The occurrence of a permanent damage is pointed out in the DC test (Figure 3-17), carried out immediately after the TLP test, and corroborated by the IV curves of the TLP tested devices, where a dramatic reduction of the maximum current flowing into the devices as well as a change in the shape with a consequent loss of their proper functionality is evident (Figure 3-16). An analysis of the post-TLP electrical features was not carried out since all the transistors tested did not keep a proper functionality.

Table 2: The TLP parameters obtained from the analysis of P3HT OFETs tested with positive drain-source pulses (DSpos) with the gate kept grounded.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.22±0.05	349±16	76.78±21.8	6.58±1.82	2.9±1.14
10 µm	0.14±0.01	284±8	39.76±4.04	3.38±0.32	2.1±0.95
5 µm	0.17±0.02	272±3	46.24±6.01	3.87±0.51	1.9±0.79

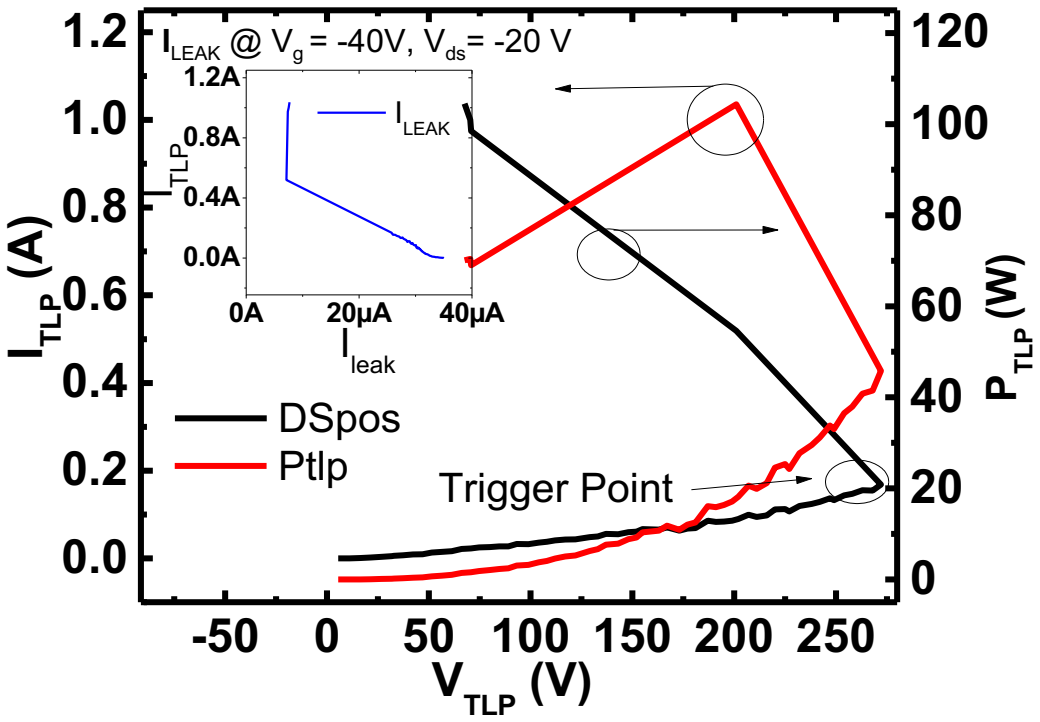


Figure 3-13: the TLP results of a 5-µm channel length transistor carried out in DSpos mode. On the right ordinate, the I_{TLP} values whilst on the left one the P_{TLP} are reported. In the inset, the I_{LEAK} graph is shown.

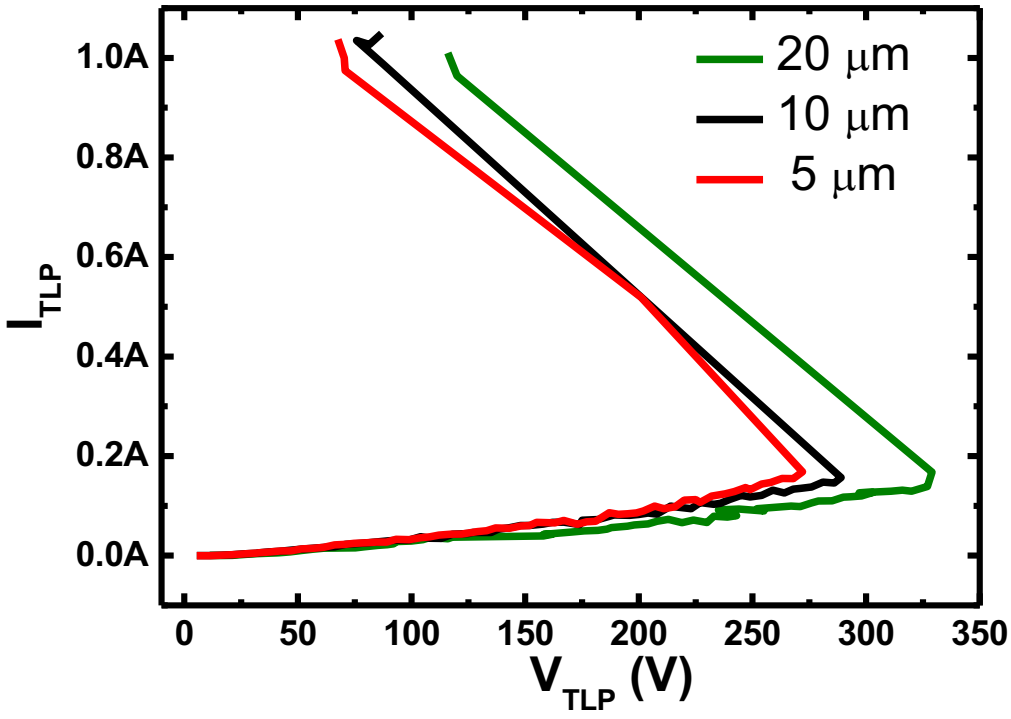


Figure 3-14: The effect of the channel length on the trigger voltage in DSpos mode tested devices. It is possible to see how the trigger point is progressively scaling according to the channel length.

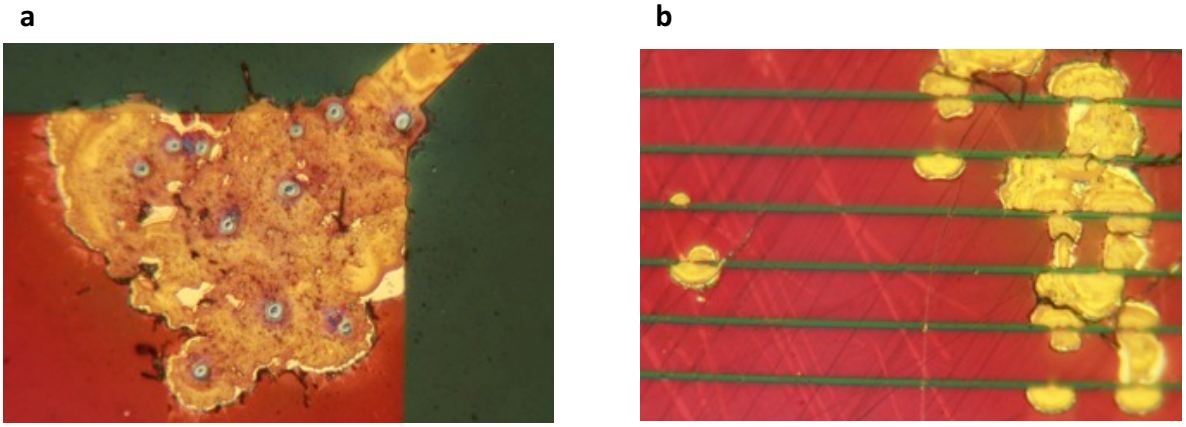


Figure 3-15: The damages due to the TLP stress on a drain contact (a) and on the interdigitated structure (b) of a transistor, tested in DSpos mode TLP. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

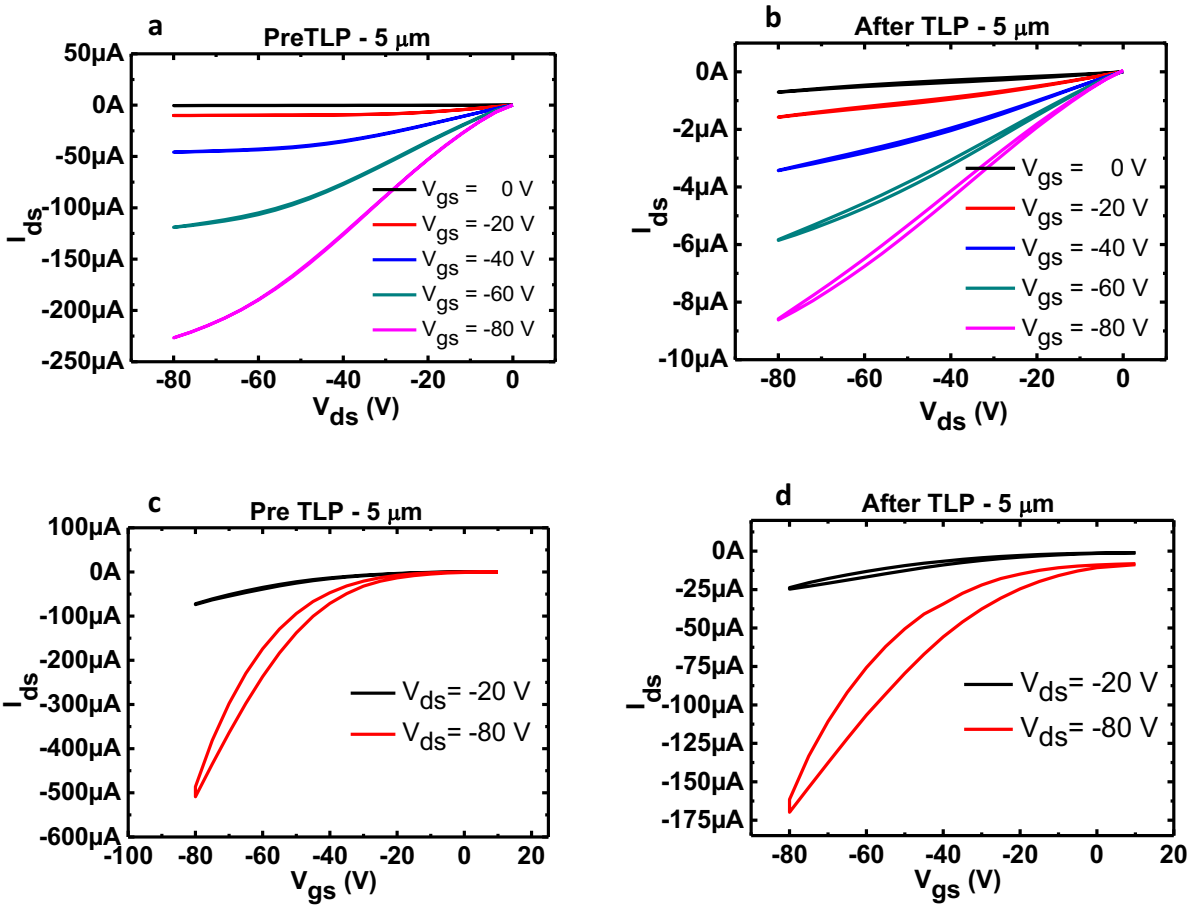


Figure 3-16: In figure a and c the pre-TLP characteristics are reported, whilst in figures b and d those registered after the TLP are shown.

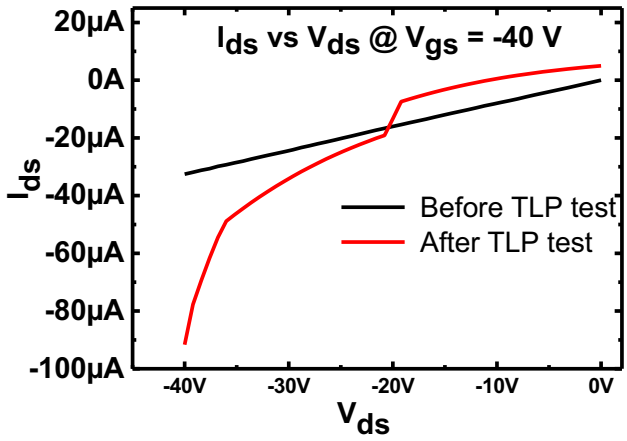


Figure 3-17: The DC test of a 5 µm-channel length. The device is damaged.

3.2.2.3.2 Negative Drain-source-no bias (DSneg)

The DSneg test did not cause the failure of the devices tested that maintained their functionality, and none of the devices failed the I_{LEAK} test, which resulted always lower than 310 µA, and thus no

Table 3: The TLP parameters obtained from the analysis of P3HT OFETs tested with negative drain-source pulses (DSneg) with the gate kept grounded.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.046±0.002	228±10.8	10.68±1.1	0.91±0.001	4.65±0.12
10 µm	0.06±0.02	240±10.2	14.34±5.63	1.23±0.5	4.67±0.11
5 µm	0.048±0.02	217±23.7	10.61±5.62	0.91±0.5	5.12±0.17

short circuits arise because of the test. However, the resulting pulsed energy measured was always lower than 2 µJ, a value lower than those observed in the DSpos, and therefore exposing these devices to a moderate ESD stress. The reason is due to the interruption of the charge flow between the TLP probes and the device caused by a localised destruction of the drain and the source contacts, interesting solely the area immediately under the TLP probe. The DC test and the IV curves confirmed that the devices were damaged only partially and locally, rather than experiencing a systemic failure, confirming a maintained functionality. However, OFETs shows lower values of charge mobility and on/off ratio and different V_{TH} after the DSneg test. The negative pulses, pushing these devices to work in quasi-reverse conditions, caused a closure of the channel and the arising of a negative barrier that naturally repelled the pulsed negative charges. Hence, the pulsed charges mostly are discharged locally over the contact area between the probe and the pad via a heating process.

The TLP parameters are reported in table 3. The mean pulse duration highlighted by the TLP system was of 91.08 ns. The R_{TLP} was found oscillating around a value between 4.6 kΩ and 5 kΩ not following a particular trend. These values are too high for the employment of P3HT OFETs as protection themselves. The TLP graphs pointed out (Figure 3-18) the occurring of several snapbacks followed by a recovery. Furthermore, looking at all channel-lengths I_{TLP} vs V_{TLP} graphs (Figure 3-19) there is no such a thing as a dependence of the trigger values from the channel lengths. Moreover, the I_{LEAK} shape is also showing a fluctuation of the impendence across the TLP probes causing sudden reductions of the registered current, followed by recovery of the same, and an overall poor linear behaviour (Figure 3-18 Inset). These results suggest a local rupture of the drain and source pads arising during the tests and not depending from the device geometrical features and only partially

interesting the rest of the device (the interdigitated pattern and the polymer). Such explanation is supported in Figure 3-20 where the curves of the DC test of the device, prior and after the DSneg, show a similar response, underlying no functionality loss. The IV curves of the devices (Figure 3-21) measured after the DSneg test show that OFETs are still working. The features of DSneg-tested OFETs are reported in Table 4. The parameters are comparable, interestingly the mobility is increased by 30 % roughly, whilst the mean value of the V_{TH} is decreased by ~ 10 % and the one of the on/off ratio is decreased by ~ 30 %. However, considering also the confidence interval, such variations are indicating that the functionality of such OFETs is mostly unchanged, confirming that the ESD stress did not cause fatal damages, albeit, from the IV curves, as confirmed by the on/off ratio parameter, a decrease of the I_{DSMAX} is evident and it is probably due to a slight reduction of the conductivity of the OFETs metal lines. From an analysis of the picture of the surface of these devices, no extended damages were found, hence confirming that the pulsed energy was mostly discharging over reduced areas of the pads (Figure 3-22), whereas the remaining part only partially caused an increase of the metal lines resistance.

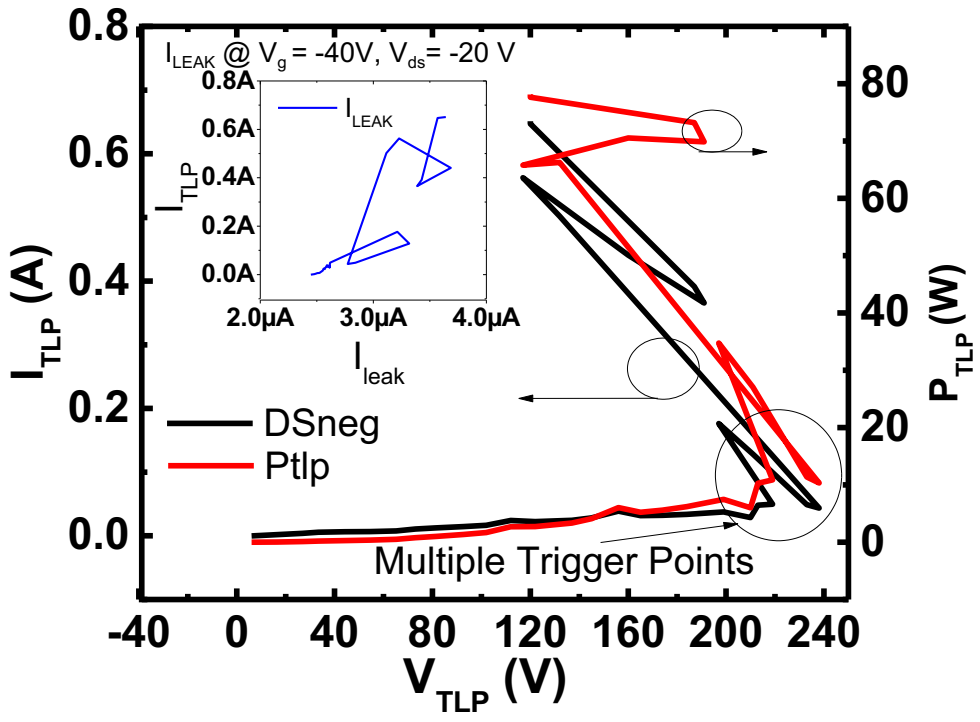


Figure 3-18: The TLP results obtained on a 20 µm channel length P3HT OFET in drain-source negative pulses modality.

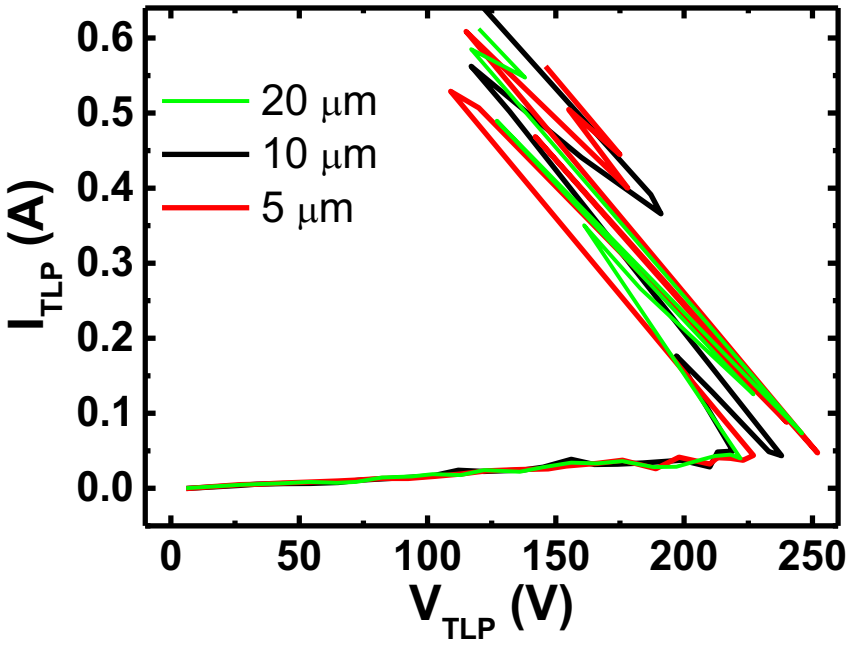


Figure 3-19: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested. Notably, a first important snapback happens around the same value of V_{TLP}, i.e. ~225 V, regardless of the channel length featured by the tested transistors.

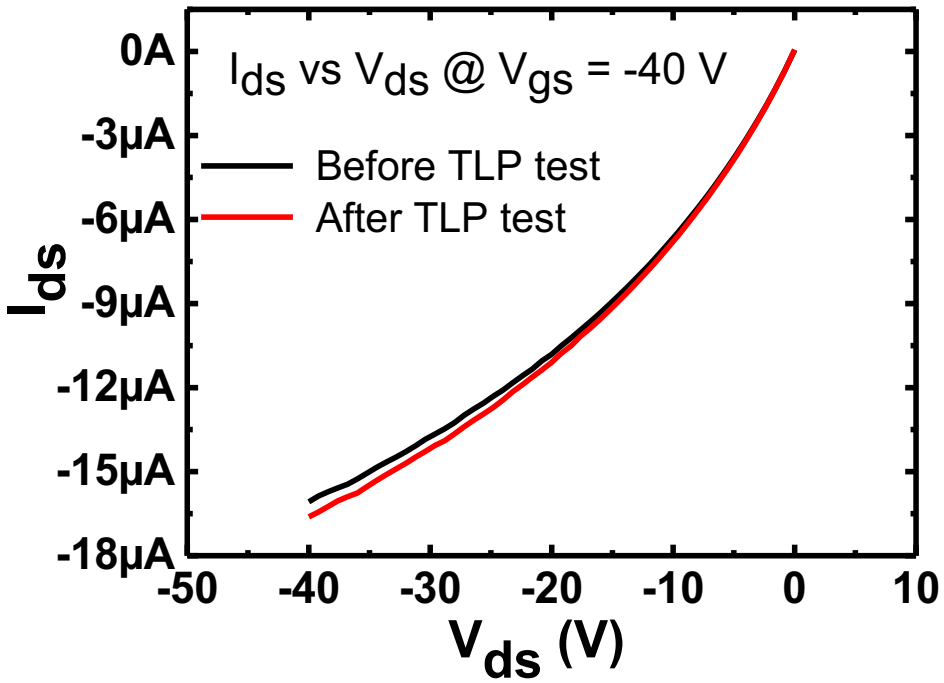


Figure 3-20: The DC behaviour of the devices before and after the negative drain-source TLP test for an applied V_{GS} equal to 0 V.

Table 4:The electrical features of the devices before and after the DSneg test. The parameters are comparable indicating that the functionality of the devices is maintained.

DUT	Mobility ($x10^{-3}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^4$)
Pristine	6.9±0.01	-17.4±5.2	0.9±0.16
Post DSneg test	6.5±0.03	-15.8±5.9	0.63±0.09

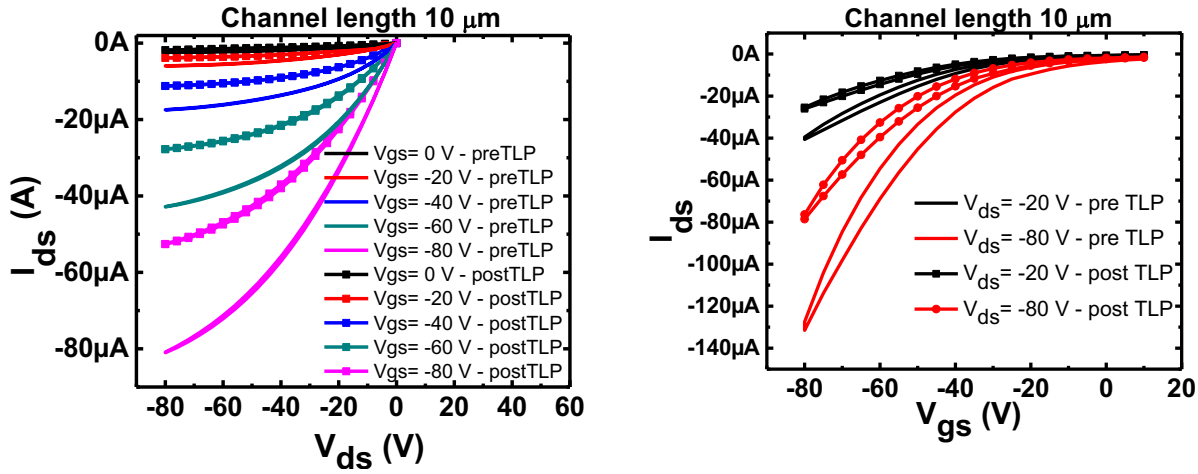


Figure 3-21: The IV curves of a 10 µm channel length OFET prior and after the DSneg test. It is possible to notice how the general functionality is maintained.

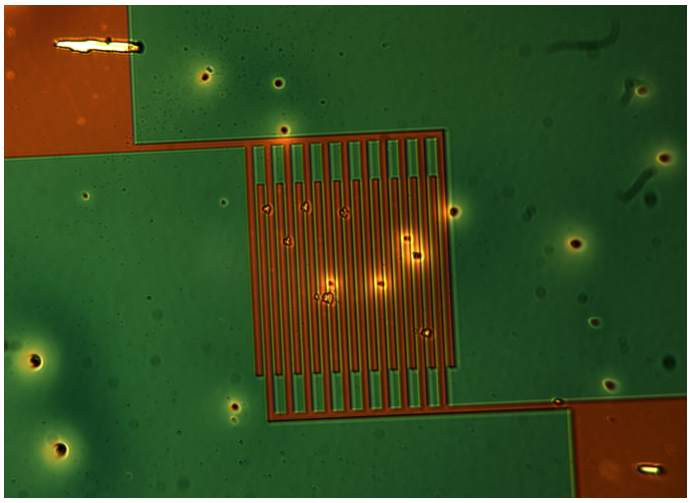


Figure 3-22: A picture of a negative DS TLP treated transistor, precisely a 5 µm-channel length one, showing no extended damages on the substrate. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 5x zoom.

.

3.2.2.3.3 Positive Drain-source-Vg bias 10 V (DSpos10V$_g$bias)

The DSpos10V$_g$bias test was fatal to all the devices in this way tested, which suffered of a complete loss of their functionality, despite that none of the devices failed the I_{FAIL} test. In fact, I_{LEAK} was found lower than 110 µA, hence no short circuits arise because of the test. In this case, the polymer is forced to work as an n-type OFETs, since the positive bias of the gate attracts negative charges. Upon an applied positive pulse, electron thin layer formed over the insulator-semiconductor interface allows positive injected pulsed charges to flow away. However, due to the slow electron mobility, a stagnation of the pulsed charges takes place, and therefore overheating of the metal lines in correspondence of the connections between the pads and the interdigitated pattern of the devices occurs leading these devices to a total failure. In fact, the device working as n-type device inefficiently drains the heat caused by the pulses.

The I_{TLP} vs V_{TLP} graphs (Figure 3-23) pointed out a clear snapback event in all devices tested. The I_{LEAK} was found to be increasing linearly during the TLP test up to the point in which the I_{TLP} reaches the I_{TRIG} value and onwards the I_{LEAK} is remaining around the same value. This behaviour stresses out an incipient damage taking place in correspondence of the trigger values, expectably affecting only a portion of the device. The TLP parameters measured respectively for the 20 µm, the 10 µm and the 5 µm channel transistors are reported in Table 5. The mean pulse duration pointed out by the system was 92 ns. R_{TLP} was found in the between of 2.9 kΩ and 2.66 kΩ. There is no a channel length effect, this can be explained taking in consideration that electron channel is poorly formed and electron mobility is low, therefore the geometrical parameters effect (Figure 3-24) on the OFETs functionality is negligible.

Table 5: The TLP parameters obtained from the analysis of P3HT OFETs tested with positive drain-source pulses applied over devices gate-biased with a 10 V voltage (DSpos10Vgbias) gate.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.11±0.015	269.7±20	29.3±6.4	2.7±0.6	2.66±0.02
10 µm	0.14±0.047	289.7±4.5	41±14.5	3.78±1.3	2.75±0.05
5 µm	0.14±0.012	292.4±6.6	41.84±4.4	3.85±0.4	2.86±0.02

Looking at the picture of the devices (Figure 3-26) we can find minor damages on the internal metal lines, whilst a break of the connection between the pads and the interdigitated pattern is visible, meaning the pulsed charges are mostly stagnating over the pad-interdigitated fingers metal connection due to the resistance pulsed charges encounter because of the slow reaction and the low electron mobility of the polymer. The loss of functionality the DC test points out (Figure 3-25) is due to such metal connection failure. I did not report the IV curves of the TLP tested OFETs, according the DSpos10$V_g$bias, since none of them maintained a reasonable transistor behaviour.

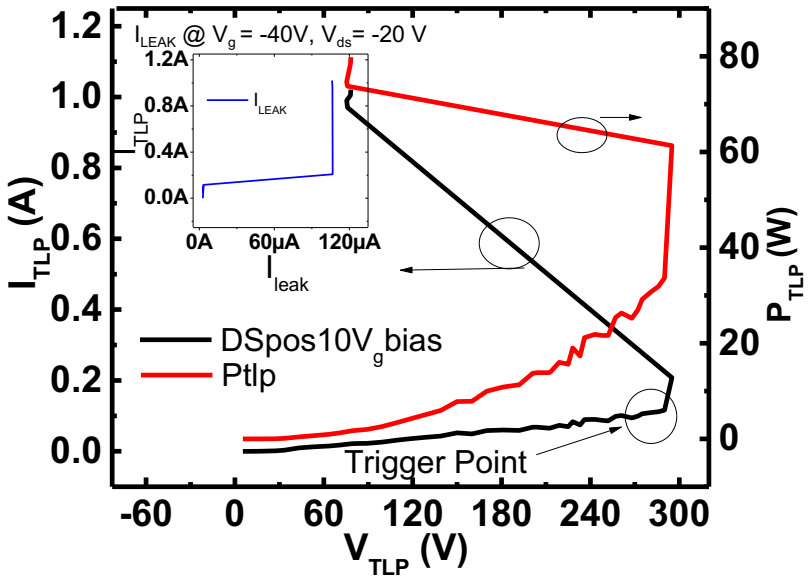


Figure 3-23: The TLP results obtained on a 10 µm channel length P3HT OFET in drain-source positive pulses-10 V bias modality.

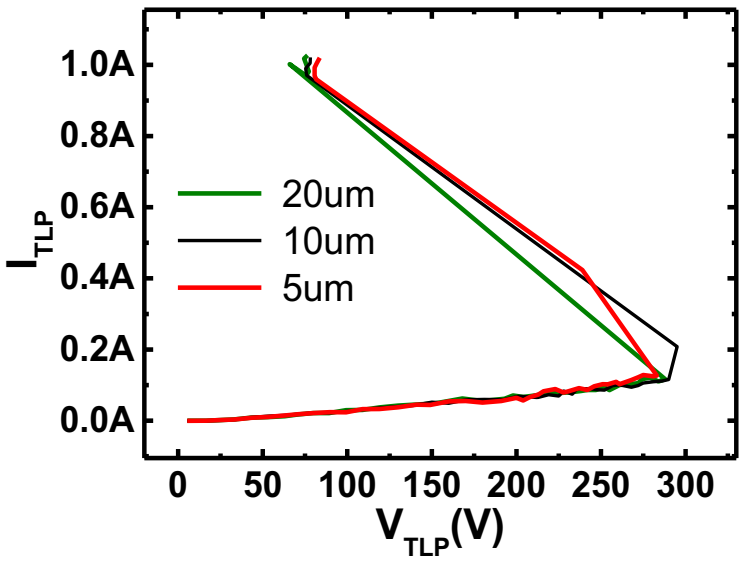


Figure 3-24: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested. Notably the snapback happens around the same V_{TLP} value regardless of the channel length featured by the tested transistors.

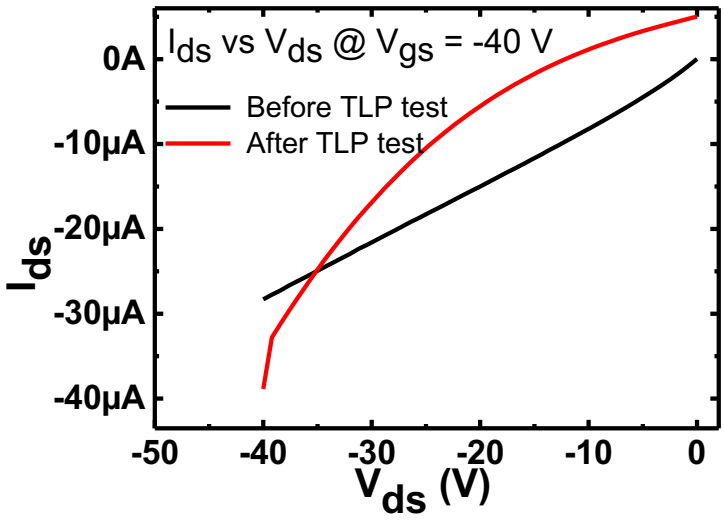


Figure 3-25: The DC behaviour of the devices before and after the negative drain-source TLP test for an applied V_{GS} equal to 10 V. The change of the behaviour shows that the test fatally compromised the devices functionality.

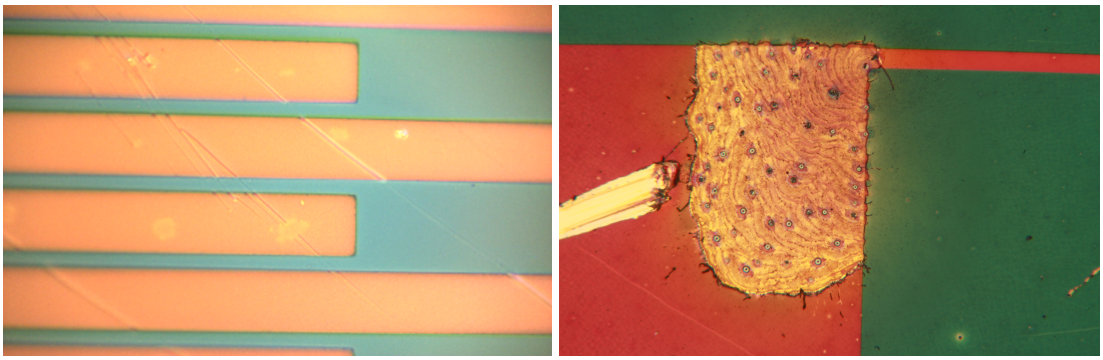


Figure 3-26: The metal lines of a 5-μm channel length P3HT OFET 10 V bias DS positive TLP treated. Only minor damages can be seen internally the device, whilst the pad suffered a total failure. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.2.3.4 Negative Drain-source-Vg bias 10 V (DSneg10V$_g$bias)

Table 6: The TLP parameters obtained from the analysis of P3HT OFETs tested with negative drain-source pulses applied over devices gate-biased with a 10 V voltage (DSneg10Vgbias) gate.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (μJ)	R_{TLP} (kΩ)
20 μm	0.05±0.004	193.3±11.8	9.7±1.4	0.87±0.13	4.1±0.44
10 μm	0.056±0.003	227.6±11.4	12.6±1.4	1.14±0.12	3.6±0.07
5 μm	0.048±0.011	245.7±3.4	12.1±3	1.08±0.27	4.3±0.78

The DSneg10$V_g$bias test did not cause a fatal damaging of tested devices (Figure 3-30). The negative injected pulsed charges cannot travel through the formed channel and, furthermore, are not favoured to travel across the rest of the polymer either since holes are spread over the upper part of the polymer, far from the insulator-semiconductor interface. Hence, the charges are mostly remaining confined locally over the TLP probe-pad area of contact, similarly to what observed in the previous case of DSneg (Figure 3-28). Such explanation justifies the several snapbacks present into the I_{TLP} vs V_{TLP} graphs, as a sign of a fluctuating charge transfer from the TLP line to the DUT. The I_{LEAK} measured was always lower than 20 µA, hence none of the failed devices overcomes the I_{FAIL} value (0.5 mA) so suffering a short circuit because of the test. The I_{TLP} vs V_{TLP} graphs (Figure 3-27) pointed out multiple snapbacks event in all devices tested according this TLP modality, confirming a fluctuating charge transfer from the TLP probe to the device. Such disruption is also underlined by the I_{LEAK} that is considerably reduced after the occurring of the snapbacks, so revealing a loss of electrical contact of the probes with the pads. The TLP parameters measured respectively for the 20 µm, the 10 µm and the5 µm are reported in Table 6. The mean duration of applied pulses is 90.8 ns. Considering these latter values if compared with those recorded for the same TLP test but with an opposite polarity of the pulses (positive pulses and 10 V_g bias) we can observe that the trigger point occurs for lower values of I_{TP} and V_{TLP} and lower values of pulsed energy. The pulsed energy was lower than 1.5 µJ, not enough for resulting fatal to the entire device. The R_{TLP} was found to range from 3.5 kΩ to 4.4 kΩ. There is no a clear channel length effect. Also, the pictures of the devices taken after test confirm there are not extended damages on the surface of the OFETs (Figure 3-29). The DC (Figure 3-30) tests and the IV curves (Figure 3-31) show OFETs still working after the DSneg10$V_g$bias test. The electrical features of these devices are reported in Table 7. The mobility remains approximately the same, whilst the mean value of the V_{TH} decreases by ∼ 10 % and the on/off ratio decreases by ∼ 33 %. The latter reduction is also visible from the IV curves post TLP test (Figure 3-31) where a decrease of the I_{DSMAX} is evident, probably due to a slight reduction of the conductivity of the OFETs metal lines or to charges remaining trapped and influencing the I_{DS}.

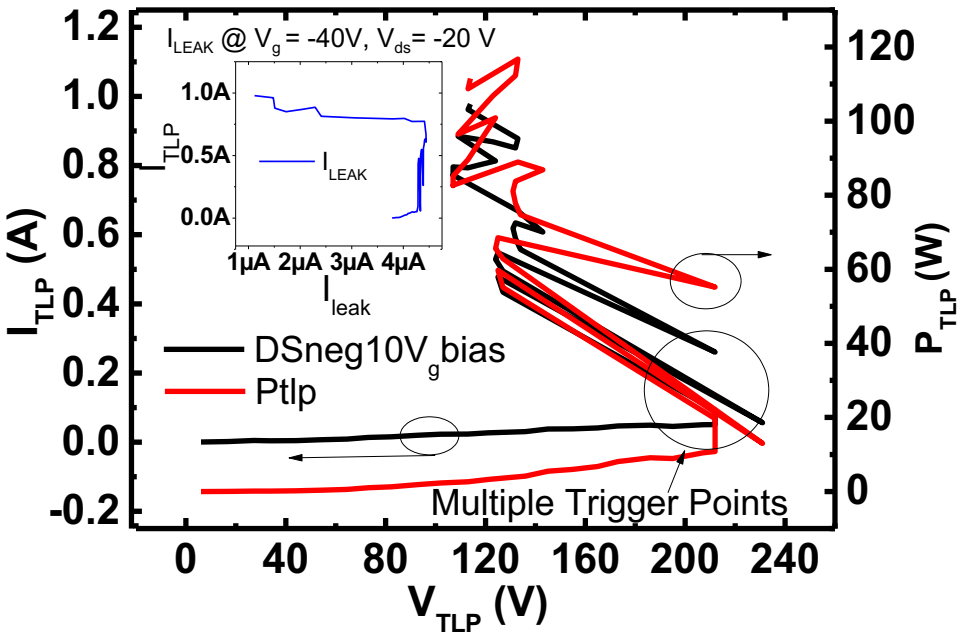


Figure 3-27: The TLP results obtained on a 10 µm channel length P3HT OFET in drain-source negative pulses 10 V bias modality.

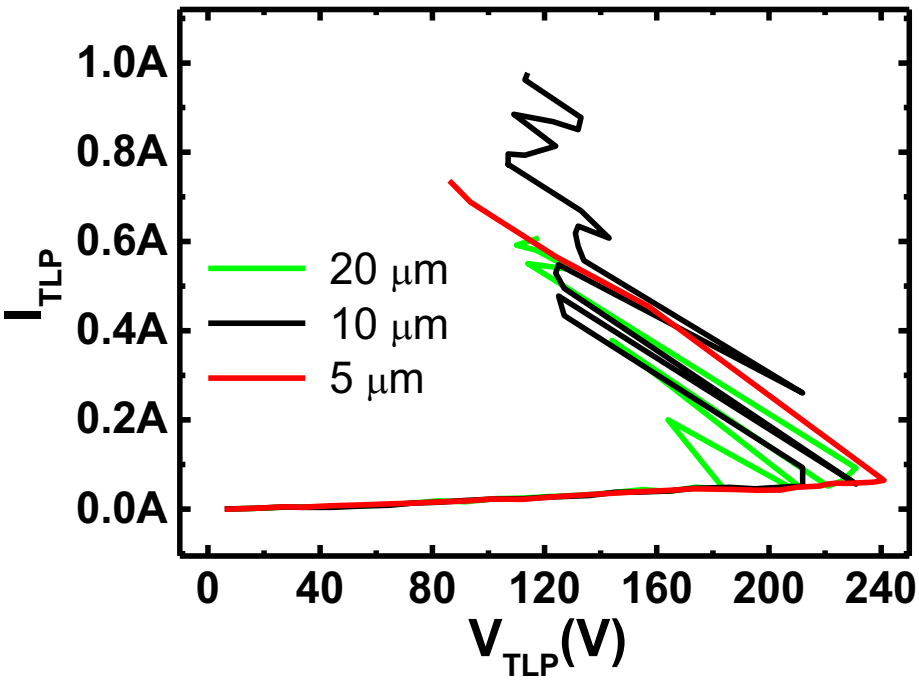


Figure 3-28: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested. Several snapbacks take place and there is no a clear channel length effect.

Table 7: The electrical features of the devices before and after the DSneg10$V_g$bias test. The parameters are very similar, stressing that only a small variation of the OFETs behaviour occurred.

DUT	Mobility ($x10^{-3}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^4$)
Pristine	5.67±0.45	-15.4±6.4	0.9±2.5
Post DSneg10$V_g$bias test	5.67±0.44	-13.8±6.2	0.6±1.6

Figure 3-29: The metal lines of a 5-µm channel length P3HT OFET 10 V bias DS negative TLP treated. No damages are highlighted. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

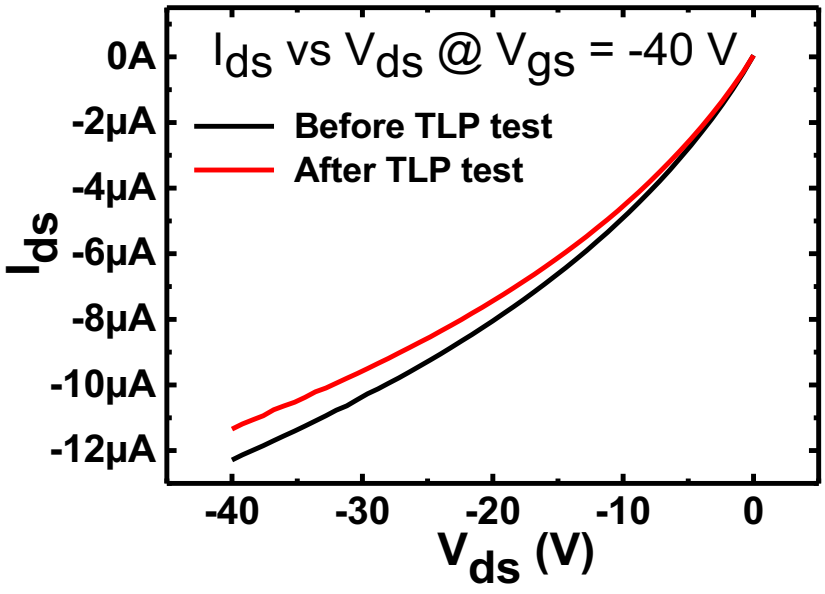


Figure 3-30: The DC behaviour of a 20-µm channel length OFET before and after the negative drain-source TLP test for an applied V_{GS} equal to 10 V.

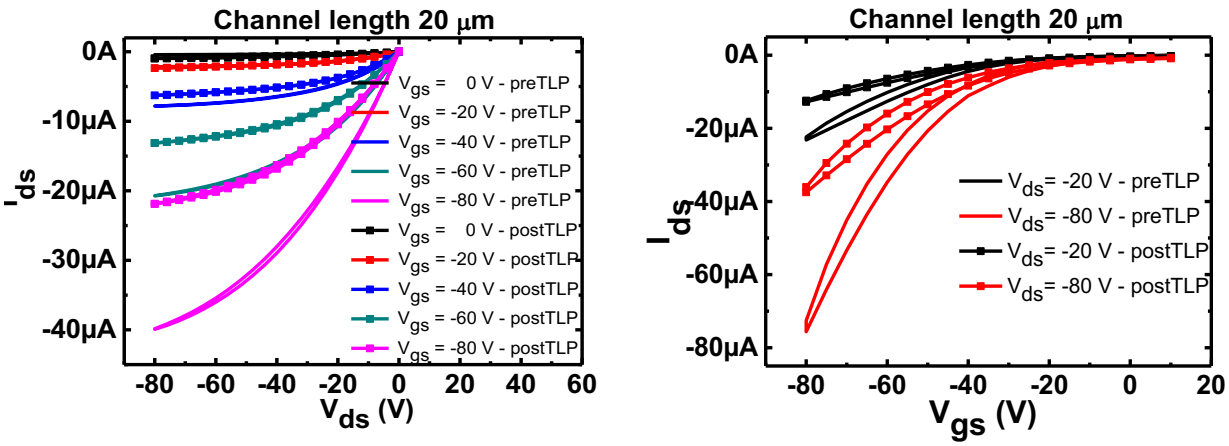


Figure 3-31: The IV curves of a 20 µm channel length OFET prior and after the DSneg10V$_g$bias test. It is possible to notice how the general functionality is maintained.

3.2.2.3.5 Positive Drain-source-Vg bias -20 (DSpos-20V$_g$bias)

The DSPos-20V$_g$bias test caused a complete loss of the functionality in all tested devices. Such failures are due to a damage of the metal lines of the device. In this configuration, the channel of transistors is opened so allowing the pulsed current to flow through the device, and thus to directly discharge over the metal lines of the device up to the point at which the latter are completely damaged. The I_{LEAK} measured was always lower than 110 µA, hence always lower than the failure leakage current, so confirming that no short-circuits arise because of the test. Furthermore, the I_{LEAK} suddenly increases after the trigger point to reach a constant value afterwards. Such behaviour stresses the fact that a substantial change of the conductance across the device is taking place. The shape can suggest that a compliance value is reached and that the systems itself is retaining the I_{LEAK} to the compliance value, but this is not the case since the compliance current for the I_{LEAK} was set to 1 mA and neither the I_{FAIL}, set to 0.5 mA, was reached. The I_{TLP} vs V_{TLP} graphs (Figure 3-32 and Figure 3-27) pointed out a clear snapback event in all tested devices according this TLP testing mode, and therefore parasitic electrical paths arising and discharging the pulsed current. The TLP parameters measured respectively for the 20 µm, the 10 µm and the 5 µm are reported in Table 8. The mean duration of the pulses is 89.2 ns. The R_{TLP} was found to be ~ 2.4 kΩ. The energy directly discharged over the metal lines of the devices is always higher than 2 µJ, a value sufficient to provide a spread damage. There is a displacement of TLP parameter values between the 20 µ-channel length OFETs and the other channel lengths, i.e. the 10 µm and the 5 µm, which feature instead similar

values (Figure 3-33), except for the R_{TLP} that is similar in all tested devices regardless of the channel length. A fatal damaging of the devices is confirmed by the DC test (Figure 3-34) and by the pictures taken after the test (Figure 3-35), pointing out spread damages throughout the device structure. I do not report any post TLP IV curve since none of the devices kept a sufficient degree of functionality to allow a meaningful analysis.

Table 8: The TLP parameters obtained from the analysis of P3HT OFETs tested with positive drain-source pulses applied over devices gate-biased with a -20 V voltage (DSpos-20Vgbias) gate.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.11±0.01	261.7±2	28.5±2	2.54±0.2	2.4±0.04
10 µm	0.11±0.02	252.7±3	28.6±5	2.56±0.5	2.4±0.12
5 µm	0.15±0.04	253±3	38.6±11	3.44±1	2.2±0.11

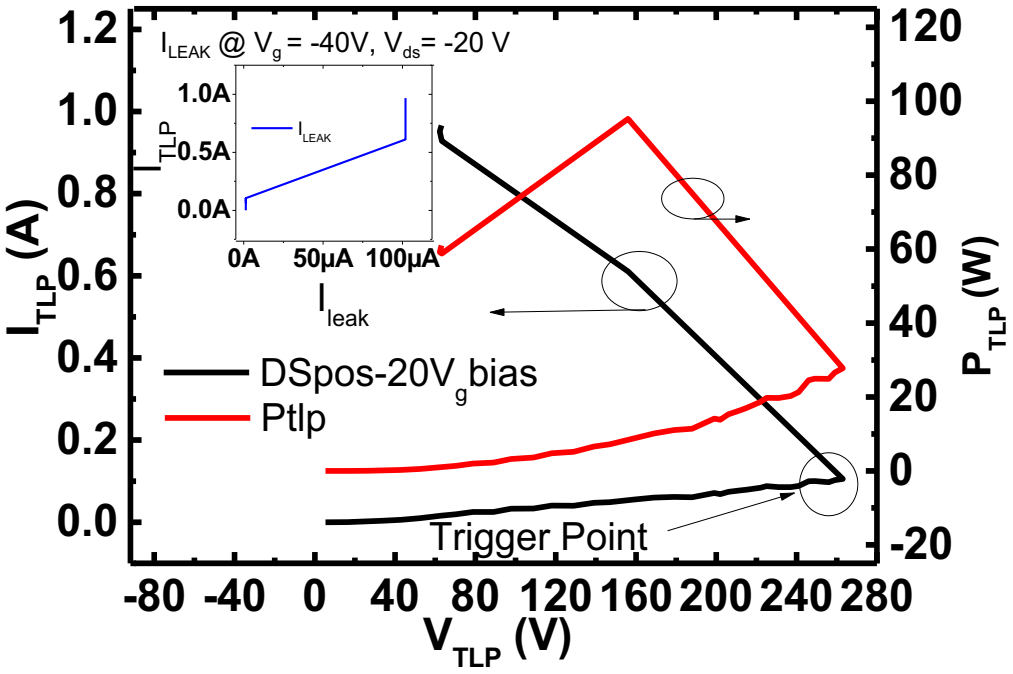


Figure 3-32: The TLP results obtained on a 20 µm channel length P3HT OFET in drain-source negative pulses-20 V bias modality.

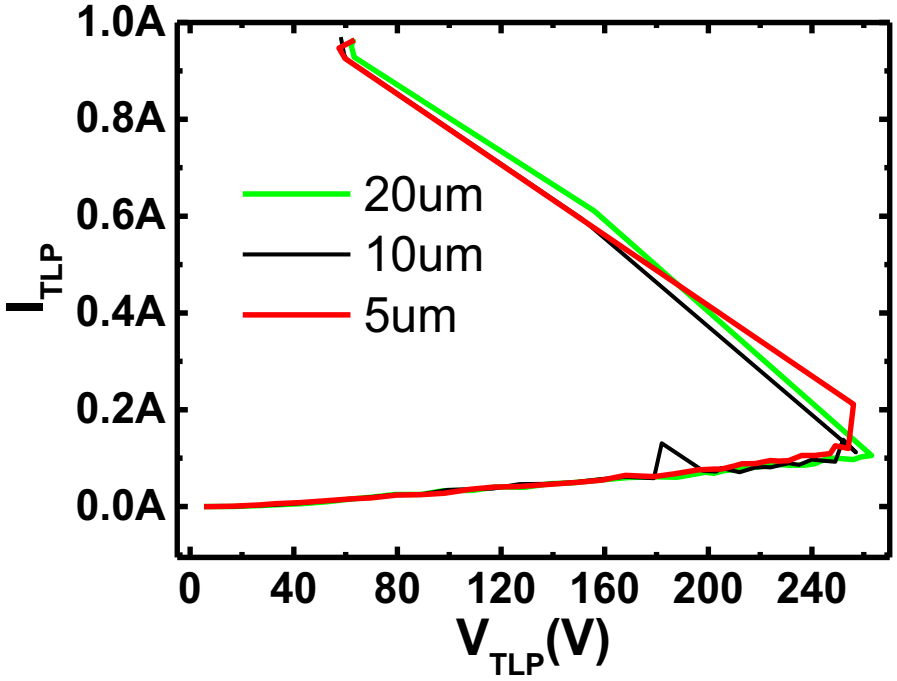


Figure 3-33: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested.

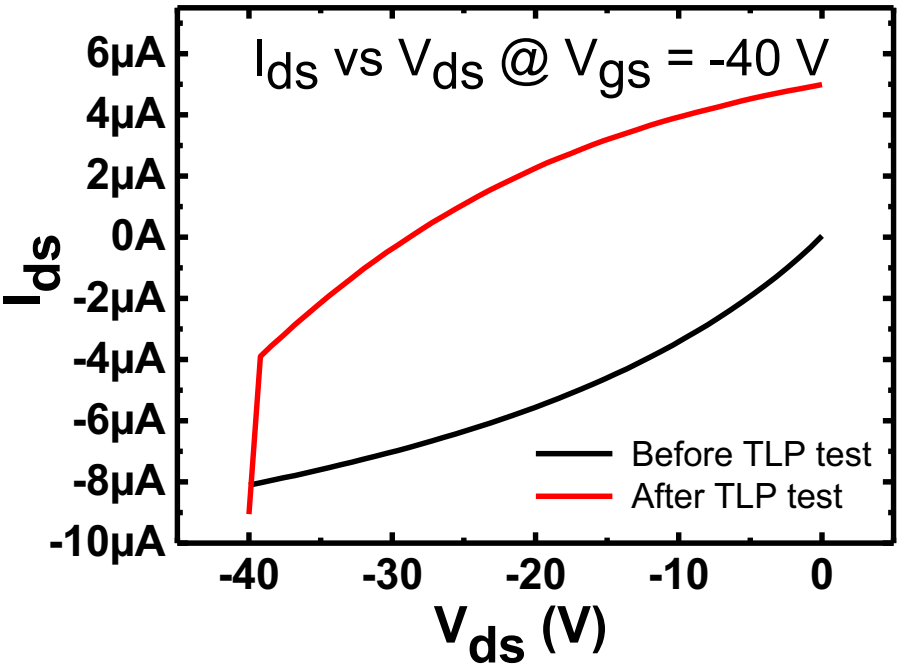


Figure 3-34: The DC behaviour of a 20-μm channel length OFET before and after the positive drain-source TLP test for an applied V_{GS} equal to -20 V.

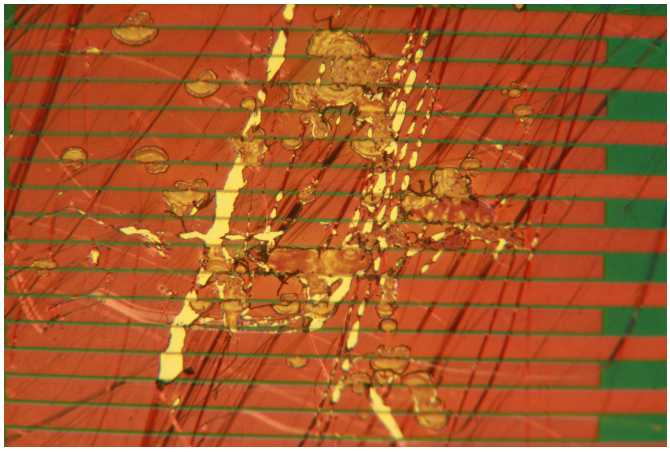


Figure 3-35: Pictures of a damaged transistor after the DSpos -20 V bias TLP. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 20x zoom.

3.2.2.3.6 Negative Drain-source-Vg bias -20V (DSneg-20$V_g$bias)

The DSneg-20$V_g$bias test did not cause a complete failure of the devices, similarly to other cases so far analysed involving negative applied pulses. The reason is due to the pulses being discharged mostly locally over the contact area between the TLP probe and the transistor pad, up to the point the electrical path between the TLP line and the DUT is disrupted. The pulsed energy is lower than 1.5 µJ (pulse mean duration of 92 ns) in all devices tested, too low to cause fatal damages to the devices. The I_{LEAK} measured was always lower than 44 µA, hence always lower than the failure leakage current and confirming that no short circuits arise due to the test. The I_{LEAK} is poorly linear as a consequence of the electrical path instability. The I_{TLP} vs V_{TLP} graphs (Figure 3-36) pointed out several snapbacks event in all devices tested according this TLP modality. These are due to a fluctuation of the electrical path stability, similarly to what already observed in the case of DSneg and DSneg10$V_g$bias, and thus confirming that negative pulses are prone to cause local damages in correspondence of the contact area between the TLP probe and the drain/source pads, rather than more spread damages over the rest of the device. The TLP parameters measured respectively for the 20 µm, the 10 µm and the 5 µm are reported in Table 9. There is not a channel length effect in the TLP response (Figure 3-37), since pulsed current is discharged locally and the channel of transistors, the behaviour of which is depending on geometrical parameters, is therefore not involved directly. The R_{TLP} ranges between 3.3 kΩ and 3.9 kΩ not following a particular trend. Pictures of the tested devices corroborate that devices external structure is not significantly altered (Figure 3-40). Furthermore, the DC test confirm functionality of the tested devices is maintained,

analogously to what observed in the other cases in which the applied pulses between the drain and the source were negative (Figure 3-38).

The IV curves, as the DC test, show the functionality is maintained after the test (Figure 3-39). However, a degradation of the OFETs electrical features is observed, reasonably due to charges remaining trapped within the device. In terms of electrical parameters (Table 10), the mobility and the threshold voltage are substantially the same, instead there is a reduction by ~ 37% of the on/off ratio.

Table 9: The TLP parameters obtained from the analysis of P3HT OFETs tested with negative drain-source pulses applied over devices gate-biased with a -20 V voltage (DSneg-20Vgbias) gate.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.062±0.008	236±6.2	14.7±2.4	1.35±0.22	3.7±0.04
10 µm	0.066±0.002	241.7±13.6	16.1±1.4	1.48±0.13	3.5±0.21
5 µm	0.062±0.002	233.7±3.7	14.5±0.8	1.33±0.07	3.8±0.08

Table 10: The electrical features of the devices before and after the DSneg-20$V_g$bias test.

DUT	Mobility ($x10^{-3}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^4$)
Pristine	4.72±3.41	-16.7±1.1	0.8±1.4
Post DSneg-20$V_g$bias test	4.69±3.43	-15.4±5.4	0.5±1.5

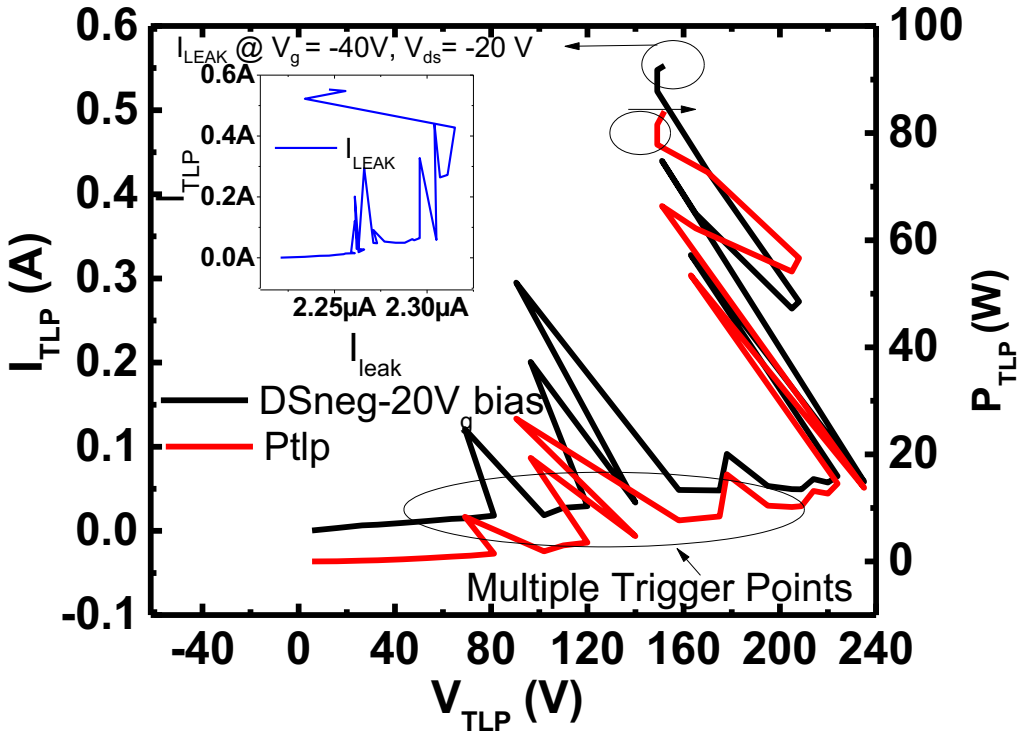


Figure 3-36: The TLP results obtained on a 10 μm channel length P3HT OFET in drain-source negative pulses-20 V_g bias mode.

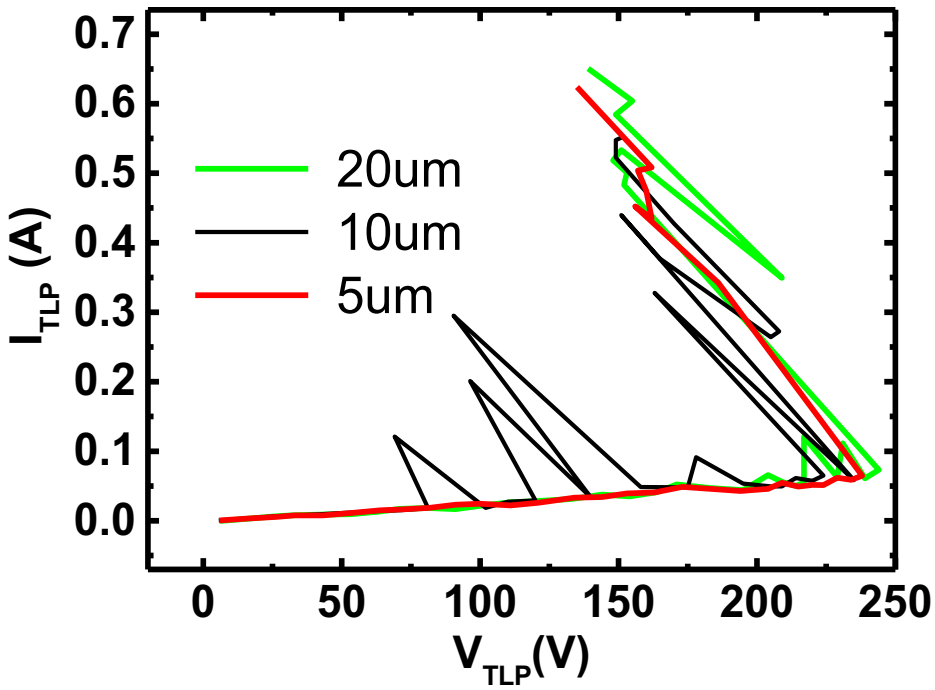


Figure 3-37: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested. Notably a clear snapback happens in spots linearly increasing in value with the channel length of transistors.

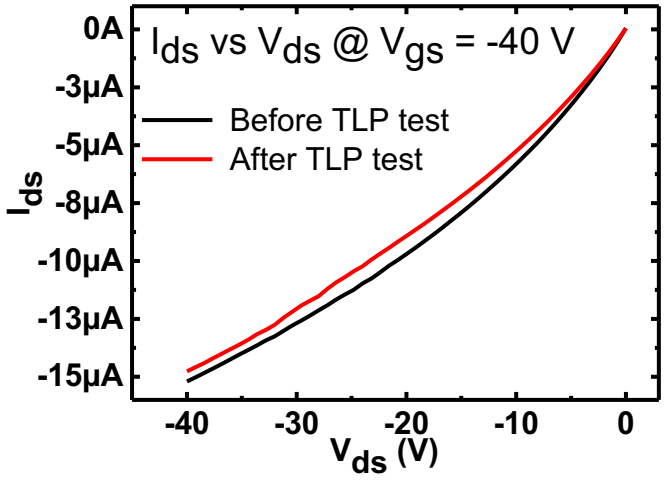


Figure 3-38 The DC behaviour of 10-μm channel length OFET before and after the positive drain-source TLP test for an applied V_{GS} equal to -20 V.

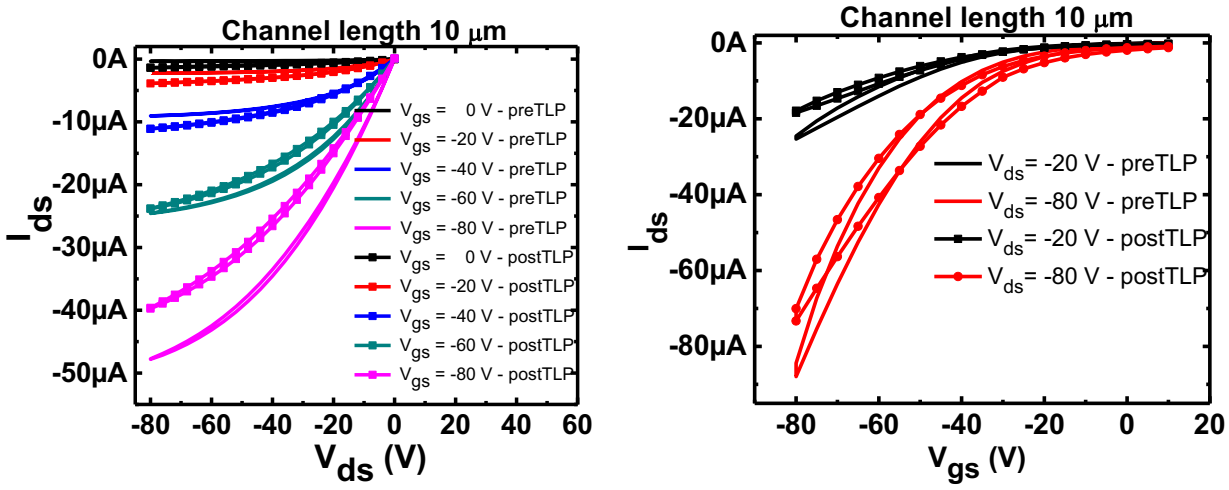


Figure 3-39: The IV curves of a 10 μm channel length OFET prior and after the DSneg-20$V_g$bias test. The devices maintain their functionality but I_{DS} currents are lower.

Figure 3-40: The metal lines of a 10-μm channel length P3HT OFET -20 V bias DS negative TLP treated. No damages are highlighted. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.2.3.7 Reduced TLP-stress DSpos test

I repeated the DSpos tests on the transistors of another chip keeping the applied pulses well below the trigger values found previously for the DSpos tests (3.2.2.3.1). This experiment aims at investigating the effects of the pulses directly on the polymer and thus on the mobility, on the voltage threshold and on the on/off ratio of the transistors. I applied TLP pulses up to a V_{TLP} of 112 V corresponding to an I_{TLP} between 0.04 A and 0.05 A in all cases, regardless of the channel length of the transistors. The mean pulse duration is 88 ns and the pulsed energy is always lower than 0.5 µJ (Table 11). In Figure 3-9a, the characteristics of a pristine 5 µm channel length transistor are reported, whilst the characteristics of the same transistor measured after the TLP-reduced stress test are reported in Figure 3-9b. The pristine values of the mobility, the V_{TH} and the on/off ratio of the transistors were found equal to 9.6 ± 1.5 $x10^{-3}$ cm^2/Vs, -17.1 ± 5.6 V and 9.6 ± 2.8$x10^6$ respectively. The same transistor, once stressed via TLP events, features a mobility of 6.3 ± 4.54$x10^{-4}$ cm^2/Vs, a V_{TH} of -19.2 ± 3.3 V and an on/off ratio of 9 ± 1.3 $x10^5$. I observed a reduction of the mobility and of the on/off ratio of approximately an order of magnitude, whereas the V_{TH} modulus increases between 17 % and 11 %. All transistors tested maintained a transistor-like behaviour.

Notably, almost all devices showed an increase of the sub-threshold current (I_{ST}) and of the hysteresis with a dramatic reduction of the I_{DSMAX} (reached for an applied V_{DS} of -80V and of V_{GS} of -80V). The reduction of the mobility is the first cause for the reduction of the I_{DSMAX}. The increases of the I_{ST} and of the hysteresis are mostly related on charges trapped within the substrate and the polymer itself suffering minor degradation. Eventually, I studied the effect of a thermal annealing on the electrical properties of the TLP-stressed devices. I annealed the TLP-tested devices at 90°C for 40 minutes in air. The IV curves measured after the annealing of the same transistor, already discussed in Figure 3-41a and b, are reported in Figure 3-9c. I observed a general improvement of the IV-curves shapes with a slight recover of the I_{DSMAX} and of the on/off ratio (~ 7 %), albeit the values of these two parameters remain in all cases approximately tenfold lower than pristine values. The I_{ST} increased after the annealing, whereas the V_{TH} modulus decreased of ~ 24 % with respect to the values measured after the TLP stress, probably due to an absorption of oxygen that is known to cause such effect[21]. Also, the annealing did not result particularly beneficial for the mobility, which still remains an order of magnitude lower than pristine values.

Table 11: The TLP parameters of the reduced TLP-stress DSpos test.

	I_{TLP} (A)	V_{TLP} (V)	P_{TLP} (W)	E_{TLP} (µJ)	R_{TLP} (kΩ)
20 µm	0.044±0.001	112±0.82	4.9±0.07	0.44±0.001	2.54±0.04
10 µm	0.046±0.003	112±0.81	5.1±0.34	0.45±0.003	2.43±0.12
5 µm	0.045±0.001	111.3±0.47	5±0.11	0.44±0.001	2.47±0.03

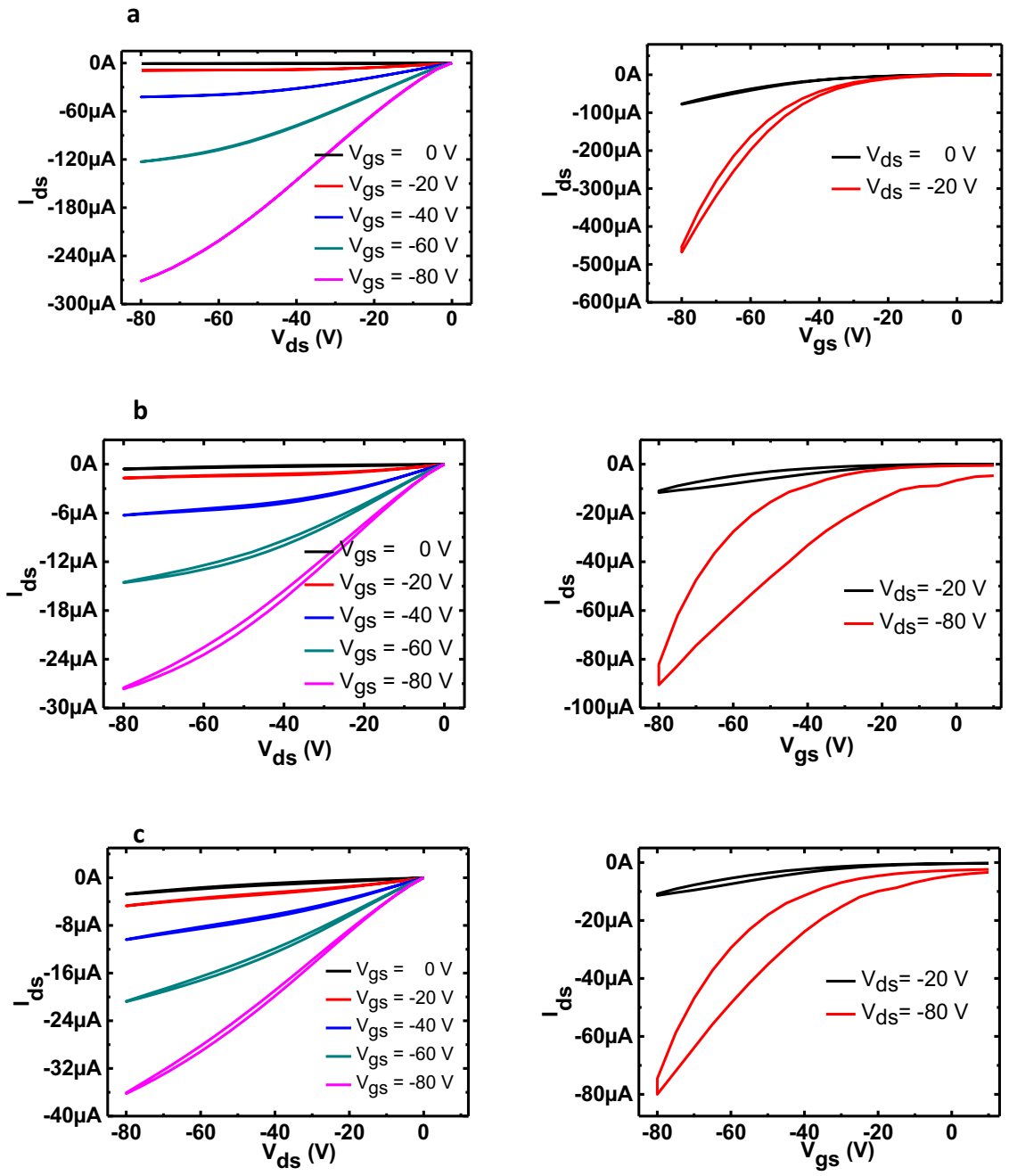
Table 12: The charge mobility, the on/off ratio and the threshold voltage measured in the P3HT transistors prior any TLP stress, after a TLP test in which the V_{TLP} was maintained lower than 112 V and after an annealing of 90° for 40 minutes. These values have been obtained from all the 16 transistors present on a substrate.

DUT	Mobility ($x10^{-3}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^3$)
Pristine	9.6 ± 1.5	-17.1 ± 5.6	9.6 ± 2.8
After TLP	0.63 ± 0.4	-19.2 ± 3.3	0.9 ± 0.1
Fresh P3HT over stressed substrate	3.1 ± 1.4	-12.71 ± 3.8	2.03 ± 0.9

The value of the charge mobility, the on/off ratio and of the V_{TH} of the transistors measured prior and after the TLP-stress (V_{TLP} up to 112 V) and after the thermal annealing are reported in Table 12, obtained from all the 16 transistors present on a single chip.

A further test was carried out to assess the TLP stress impact on these devices. I washed away P3HT from the TLP stressed samples by means of a sonication bath in acetone and another one in chlorobenzene, both during 10 mins, and built new P3HT OFETs using fresh P3HT over the partially stressed substrates (Figure 3-41d). The electrical characteristics are reported in Table 12. If compared with those measured out of the pristine devices, a general loss of the features takes place

and I can assume that such worsening is very likely due to the substrate that was evidently damaged during the TLP reduced-stress test, and thus showing how the permanent damaging of these takes place for pulsed energy even lower than 0.5 μJ. Such observation is corroborated by the fact that if substrates used to fabricate OFETs are washed and reused to fabricate other OFETs the latter perform similarly.



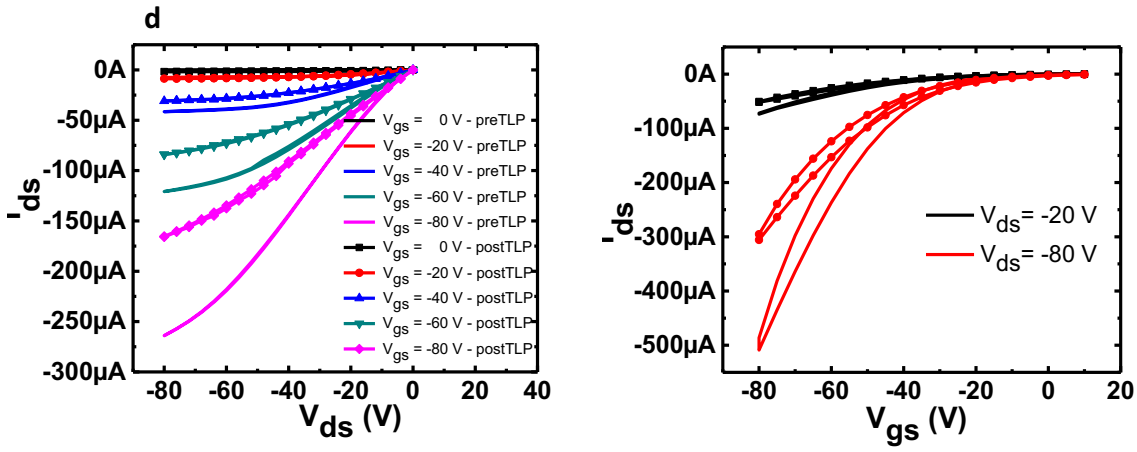


Figure 3-41: a) The output and transfer characteristic of a 5-μm channel length transistor prior the TLP test. b) The output and transfer characteristic of a 5-μm channel length transistor after a TLP test in which the V_{TLP} was maintained lower than 112 V. c) The output and transfer characteristic of a 5-μm channel length after a TLP test (V_{TLP} up to 112 V) and a thermal annealing at 90° for 40 minutes. d) The IV curves of a 5-μm channel length transistor (straight line) measured before any TLP test and of a 5-μm channel length transistor (dashed line) obtained by using fresh P3HT over a previously TLP stressed substrates.

3.2.2.4 *Raman spectra of the TLP tested P3HT OFETs*

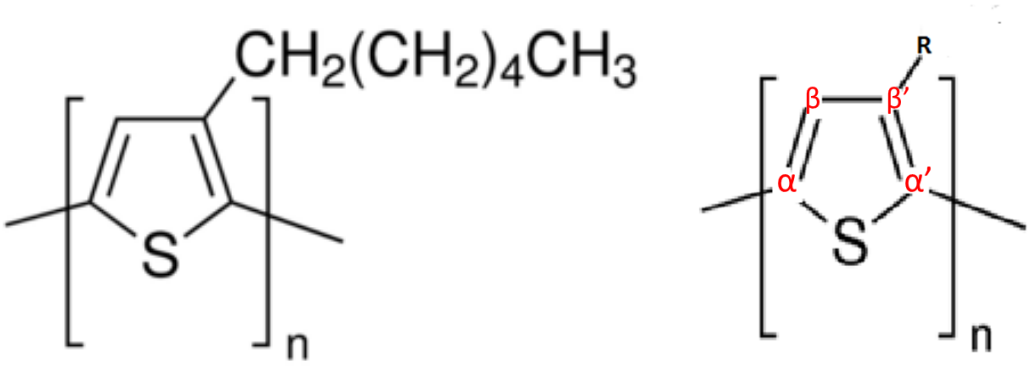


Figure 3-42: The P3HT molecular structure (left) and C positions within the thiophene ring (right).

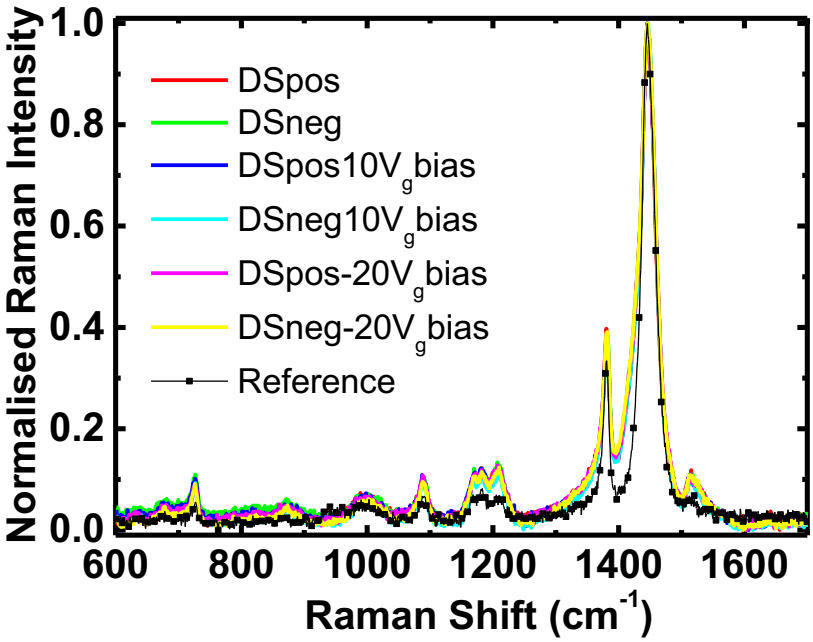


Figure 3-43: The normalised Raman spectra, within the range 600-1700 cm^{-1}, of P3HT OFETs. Spectra were collected from all the TLP-tested devices and compared to those collected from pristine ones.

The Raman spectra were collected from each of the tested devices and compared with reference spectra taken from a pristine device, namely built within the same fabrication session of the other ones and according to the same procedure and by using the very same materials, by focusing the laser beam over an area located in the middle of two metal lines of the interdigitated pattern of a 10 µm channel length. The spectra are normalised with respect to the peak at 1445 cm^{-1}, generated in P3HT spectra by the stretching of the in plane double bond C=C (C_α=C_β stretching). A representative spectrum per each TLP case was chosen and in Figure 3-43 reported. Such graph is then split in two other graphs, in the first one the portion 1300 to 1550 cm^{-1} of the original spectra is analysed (Figure 3-43 above) whilst the portion 600 to 1300 cm^{-1} is analysed in the second one (Figure 3-44 below). The vibrations of the molecular bonding are described also referring to the α- and β- positions[166] of carbons within the thiophene rings composing the polymer (Figure 3-42).

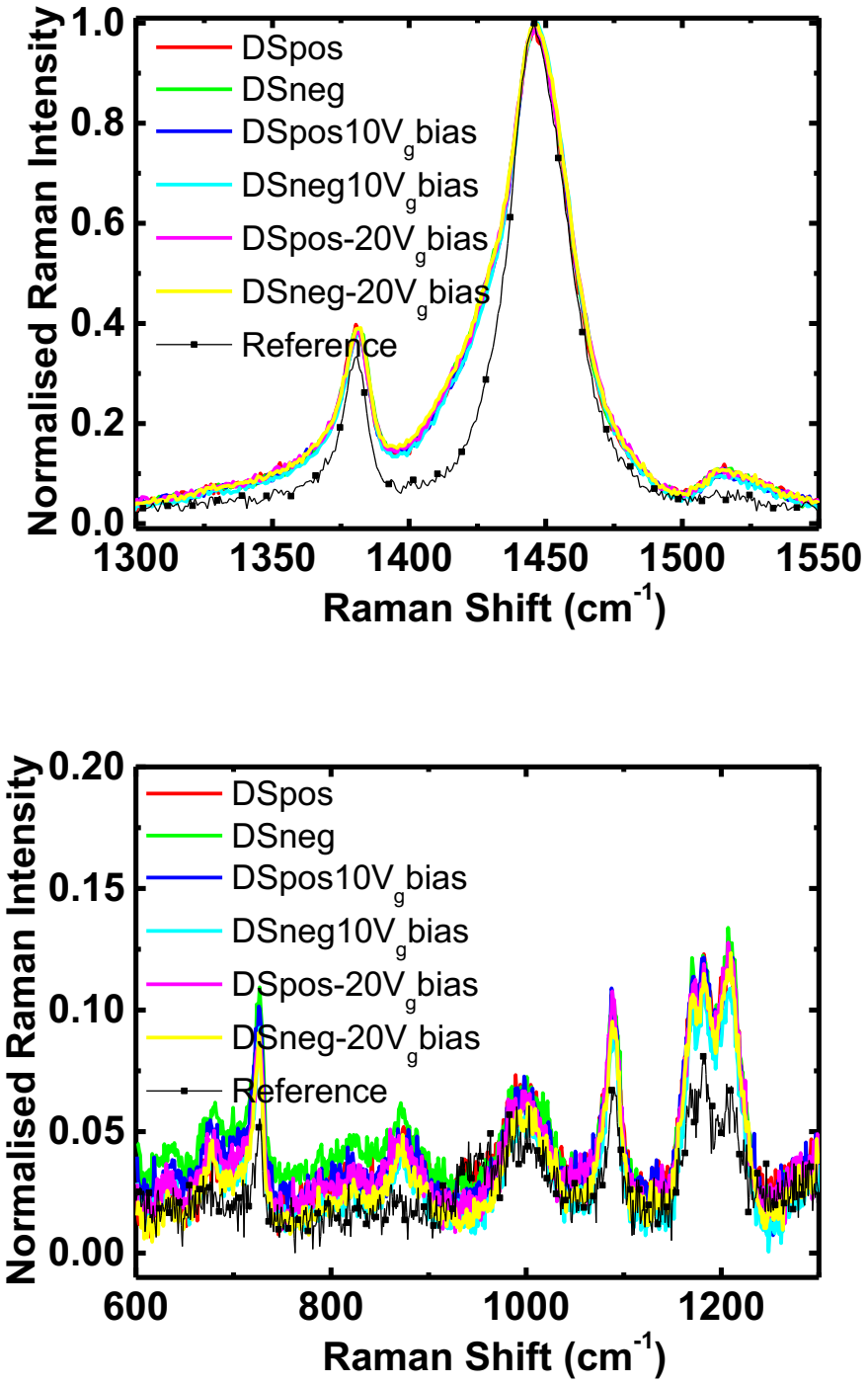


Figure 3-44: The 1300-1550 cm^{-1} (above) and the 600-1300 cm^{-1} (below) portions of the Raman spectra of the TLP tested P3HT OFETs

The portion 1300-1550 cm^{-1} is characterised by the symmetric stretch of the C=C in-plane ring mode at 1445 cm^{-1} (C_α=C_β stretching), by the C-C intraring stretch mode at 1381 cm^{-1} (C_β-$C_{\beta'}$ stretching) and by the C=C anti-symmetric stretch at 1515 cm^{-1} ($C_{\alpha'}$=$C_{\beta'}$ stretching)[10], [137], [166]. This region of the P3HT Raman spectrum is known to be sensitive to π-electron delocalisation and structural

order degradation. From Figure 3-44 it is possible to distinguish these three peaks. The portion 600-1300 cm^{-1} is characterised by a C-C inter-ring stretch mode (C_α-$C_{\alpha'}$ stretching) at 1208 cm^{-1}, by a C-H bending (C_β-H bending) at 1090 cm^{-1} and at 1182 cm^{-1}, by a C-C_{alkyl} stretch mode ($C_{\beta'}$-C_{alkyl} stretching) at 997 cm^{-1}, a C-S-C (C_α-S-$C_{\alpha'}$) deformation mode at 724 $cm^{-1}$and at 683 cm^{-1}. These peaks are visible in Figure 3-44.

From the analysis of the portion 1300-1550 cm^{-1} it is possible to see the peak at 1445 cm^{-1} appears significantly broader in comparison with the pristine one in all the spectra collected from the TLP tested devices. Such variations can be ascribed to a decrease of the molecular order and of the conjugation length in poly(thiophene) rings as effect of the TLP tests, regardless of the pulse polarisation or the gate bias applied. The peak at 1381 cm^{-1} is known to be relatively insensitive to any molecular order variation[137]. Interestingly, the peak at 1515 cm^{-1} results enhanced and broader in the spectra collected from the DSpos, the DSpos10$V_g$bias, the DSpos-20$V_g$bias and the DSneg, whereas is unaltered in the DSneg10$V_g$bias and the DSneg-20$V_g$bias tests. Such alterations can be ascribed to a formation of non-coplanar segments in the chains[10] and such explanation is corroborated by the enhancement of the 1210 cm^{-1} and 728 cm^{-1} peaks that can be observed in the portion 600-1300 cm^{-1}. These three peaks enhancements points out an induced torsional disorder along the polymer backbone due to higher disorder degree that TLP caused. Although the DSneg10$V_g$bias and DSneg-20V_g spectra were not resulting significantly altered in the 1515 cm^{-1} peak, they are in the 1210 cm^{-1} and 728 cm^{-1} ones, therefore confirming that these two TLP test modalities generate non-coplanar segments into polymer chains, as observed in the other TLP tested devices. The peak at 683 cm^{-1} also results enhanced in all cases and it is reasonably linked with that one at 728 cm^{-1} since, as the latter, is due to the C-S-C deformation and its enhancement stresses out that a higher level of induced torsional disorder is reached. The induced torsional stress on P3HT chains justifies the enhancement observed in the 997 cm^{-1} peaks, due to a higher stretch of the C-C_{alkyl}.

An enhancement of the 1182 cm^{-1} peak is also observed in TLP tested spectra. In the literature such a peak is particularly pronounced in low-doped or de-doped P3HT samples[167]. Natural de-doping of P3HT is expected to take place with time due to the instability of the P3HT, especially because of the presence of the alkyl groups alongside the chains, and can be favoured by temperature and humidity. However, reference spectra collected from samples fabricated within the same fabrication session, stored in analogous conditions and analysed with the Raman spectroscope at the same time of those TLP-stressed feature a lower peak in this point of the Raman spectra, hence

the TLP test acts as catalyser for such de-doping process. Interestingly, this interpretation also justifies the formation of the peak at 870 cm^{-1} arisen in TLP tested devices spectra, absent in the reference spectra. Such peak is reported to be directly linked to the natural stabilisation of dication species [167], [168] with time. Such process normally takes place in P3HT films over an extended period of time and it is correlated with other phenomena, such as the de-doping. Therefore, all considered, TLP tests force the whole de-doping and dication stabilisation processes to take place in a relatively short period of time acting as catalyser to these.

3.2.2.5 *Discussion over the Drain-Source TLP test results of P3HT OFETs*

The TLP test carried out over the P3HT OFETs give meaningful insights about the response to ESD phenomena of such devices. The TLP parameters highlight the strong dependence of the devices response on the pulse polarity used. The DSpos, the DSpos10$V_g$bias and the DSpos-20$V_g$bias resulted more damaging of the corresponding opposites in polarity, namely DSneg, DSneg10$V_g$bias and DSneg-20$V_g$bias. The E_{TR} measured in tests involving positive pulses was found ranging between 8 µJ and 2 µJ. Hence, any pulsed energy equal to, or higher than, 2 µJ causes an overheating of the metal lines and a fatal damaging of these. The I_{LEAK} behaviour in correspondence of the trigger point was observed to be mainly of two kinds: (i) its value plummets as a consequence of the rupture of the pad-interdigitated pattern connection; (ii) its value snaps towards higher values and tend to remain constant afterwards, stressing out that the damaging is mostly interesting the interdigitated pattern of the transistors. Whilst both i and ii failure dynamics were observed in the DSpos tests, i was the most observed in DSpos10$V_g$bias and ii the most observed in the DSpos-20$V_g$bias. None of the device resulted short-circuited by the positive pulses, reasonably due to the metal lines not physically close enough to each other to be melted upon heat exposure and. However, such metal line proximity reasonably favours metal lines to act as parasitic (not real) short-circuited capacitor in correspondence of the frequency domain (GHz) the TLP forces the devices to deal with during a discharge. This explanation justifies the snapback behaviour these devices point out.

The tests involving pulses with negative polarity were characterised by a pulsed energy ranging from 0.4 µJ to 1.8 µJ. This level of pulsed energy did not cause visible damages to the transistor metal lines, only localised damages of the area between the TLP probe and the pad, hence an area of approximately 1 mm^2. The I_{LEAK} in these tends to follow linearly the I_{TLP} up to the trigger point, meaning that at each pulse, since the very first one applied, the TLP-pad contact decreases its conductance and the I_{LEAK} encounters a progressively increasing resistance across the DUT. After the

trigger point, the I_{LEAK} loses a linear behaviour as a consequence of the instability of the electrical contact between the TLP probes and the pads. The devices tested in such modality do not lose their functionality. However, the TLP test resulted detrimental for such devices that feature worsened electrical parameters (charge mobility, on/off ratio, threshold voltage) afterwards. The mobility of these devices is reduced up to the 6%. The threshold voltage module is instead lowered in all cases of a percentage spanning between the 14% and the 7%, remaining negative, whilst the on/off ratio is lowered of a percentage ranging between the 37% and the 33% percentage. These alterations can be ascribed to both a spoiling of the semiconductor, as observed in the Raman spectra, and to an increasing of trapped charges within the device. Although pictures of the devices undergone negative pulses do not show superficial damages, the test carried out to study the effect of a reduced level of TLP stress, namely by using a pulsed energy lower than 0.45 μJ (3.2.2.3.7) and keeping the I_{TLP} lower than 0.045 A, which is almost the same value of the registered I_{TRIG} in the negative pulsed devices, confirmed that substrates are partially ruined by the TLP stress reached in the negative pulse tests. The reduction of the mobility is most probably a consequence of a higher degree of disorder caused in the polymer chains by the negative pulses, as observed from the Raman spectra (3.2.2.4). The spoiling of both the polymers and the substrates enhance the presence of traps for charges so causing the on/off reduction and the threshold voltage shift observed[99]. Charges can be trapped: (i) at the interface between the P3HT and the substrate, so generating “interface-trapped charges”; (ii) internally to the oxide close to the channel so generating “fixed charges in oxide”; (iii) at the bulk of the oxide, so generating “trapped charges in oxide”; (iv) small alkali metal such as H^+ charges or dications create “mobile trapped charges in oxide” by diffusing in it. Traps i and ii are normally introduced by structural defects that, as seen, are induced by the TLP stress. These traps are responsible for the increase of the subthreshold voltage and the concomitant lowering of the on/off ratio. The traps iii are generally formed during the fabrication process and filled during the device operations, however, the extreme conditions these devices are forced to deal with during the TLP tests justify a further injection of charges within oxide-bulk traps. The traps iv are expectably filled upon the dications stabilisation[169] process stimulated by the TLP stress as observed in the Raman spectra. The observed shift of the threshold voltage is therefore caused by the increased number of charges trapped in both the iii and iv traps.

The discriminant factor causing the devices to react as described so far is due to the position of charges within the polymer at the moment of the pulse striking. The position of the charges is depending on the applied voltage on the gate. When the gate is grounded charges within the

polymer are evenly distributed, the depletion region is expanded over a larger area than the case in which there is an applied field. Upon pulsed positive charges an applied horizontal (between the drain and the source) field takes place between drain and source[105]. The same happens between the gate and the drain in which a vertical field instead takes place. To flow through the semiconductor, the pulsed horizontal field must overcome the vertical one and this explains the channel length effect, since a shorter channel requires lower values of pulsed current to generate a horizontal field able to overcome the vertical one. Furthermore, the need to move charges according to the pulsed field, limiting at each replica the stimulus for a period of time of approximately 100 ns, determines the trigger point to take place for higher values of I_{TLP} and V_{TLP} in this TLP mode, as observed in the DSpos test.

If the gate is biased with a positive voltage, as shown in the DSpos10Vbias test, electrons are attracted to the gate and holes are moved towards the drain and the source. Upon applied pulsed current with positive polarity, the electrons at the insulator interface only partially discharge such current, hence the pulsed energy is not efficiently dissipated and metal lines start heating up. When the device reaches the trigger point a release of energy, principally because of parasitic phenomena taking place within the device, occurs causing the total failure of the device. Although the channel length affects the process reducing the required level of pulsed current to trigger such breakdown, the effect is not so evident as before for the DSpos test. Upon an applied voltage of -20 V to the gate, the channel is open and positive pulsed charges are free to pass through the polymer. The so generated current is such to destroy the metal lines of the transistors. There is a channel length effect but it is not as evident as it was in the DSpos test. The reason of the weaker channel length effect in the DSpos10$V_g$bias and in the DSpos-20$V_g$bias tests with respect to the DSpos test lies in the presence of a stable applied perpendicular field in these ones stabilising the positions of the charge carriers into the polymer between a TLP replica and another, differently to what observed in the DSpos test in which the stimulated perpendicular field is concomitant to the striking pulse only and between a replica and another charges are free to move to a more even distribution.

Upon negative pulses, regardless of the applied bias to the gate, the pulsed charges are mostly locally confined and dissipated over the limited portion of the source pad area delimited by the TLP probe. The consequent overheating causes the interruption of the electric contact between the device and the TLP system. The position of the trigger point is lower than the one observed in the previous cases. Although such consequences are common to all treated cases of applied negative pulses, the dynamics leading to them are different. In the DSneg test, since P3HT is characterised by

a higher hole mobility than the electron one, upon applied negative pulses the horizontal field is not able to overcome the vertical one, therefore the semiconductor imposes a quasi-barrier due to a slow reaction of his charge carriers. The pulsed current is therefore resulting mostly confined over the drain pad. When the gate is biased with a positive voltage, upon applied negative pulses, the polymer does not allow a net flow of charges through and the pulsed applied field is promptly annihilated by the positive charges concentrated around the drain contact. This generates a local confinement of the pulsed charges. In the case of an applied negative gate-bias, the negative pulsed charges are instead affected by the barrier taking place because of the electrons concentrated in correspondence of the drain and the source contacts. Such barrier forces these charges to mostly be locally dissipated. The trigger points found in correspondence of the DSneg, DSneg10$V_g$bias and DSneg-20$V_g$bias are similar and are defined by the metal pad itself that is able to withstand a maximum value of roughly 1.5 μJ over a localised area of approximately 1 mm^2.

Interestingly, R_{TLP} in correspondence of positive pulses is generally lower than the value found in correspondence of negative pulses. In fact, for the DSpos, the DSpos10$V_g$bias and the DSpos-20$V_g$bias the R_{TLP} is always lower than 4 kΩ and the highest values were found for the DSpos (~3.9 kΩ), coherently with what said concerning DSpos being the case requiring the highest applied pulsed field to push the device towards the trigger point. However, the displacement of the values for R_{TLP} in the DSpos case is greater than the other two cases (DSpos10$V_g$bias, DSpos-20$V_g$bias), in which R_{TLP} values are short ranged (±hundreds of Ω) around ~2.7 kΩ in the DSpos10$V_g$bias test and around ~2.4 kΩ in the DSpos-20$V_g$bias and lower than 3 kΩ in both cases. For negative pulses, the R_{TLP} was found to range between 5.3 kΩ (DSneg) and 3.3 kΩ (DSpos-20$V_g$bias), hence higher than the ones observed for positive applied pulses, as expected. Such values of R_{TLP} underline that P3HT cannot be used as ESD protection. On the contrary, protections must be designed and based on the TLP parameters this analysis pointed out, therefore taking in account that permanent damages to the devices take place starting from a pulsed energy of 0.7 μJ and that the I_{TLP} and the V_{TLP} are required to be lower than 0.037 A and 181 V, respectively. A proper design of ESD protections is beyond the aims of this thesis

Raman spectra confirmed that TLP causes a damage of the P3HT polymer in correspondence of every TLP test causing a general worsening of the molecular organization degree due to the formation of non-coplanar segments. Furthermore, an acceleration in the formation of dications groups and subsequent stabilization of the same is also observed. Signs of an early de-doping taking place process were also observed.

3.2.3 **TLP results on PBTTT OFETs**

I prepared PBTTT based OFETs to assess the response to ESD phenomena of such devices. In this section, I report on the results obtained for the TLP treated PBTTT OFETs.

3.2.3.1 ***PBTTT Drain-Gate TLP-tests***

The drain-gate tests in both polarities (DGpos and DGneg) are carried out keeping the source floating, uniquely involving the gate oxide, i.e. the insulator of the devices. The results found for P3HT OFETs are valid for PBTTT ones as well, since the polymer is not involved and the insulator of the devices are identical in both devices (see 3.2.2.1 and 3.2.2.2).

3.2.3.2 ***PBTTT Drain-Source TLP test***

I carried out the drain-source tests (DSpos and DSneg) according to the same modalities previously presented, namely: (i)drain-source in both polarities with the gate grounded (DSpos and DSneg); (ii) drain-source in both polarities with an applied bias of 10 V on the gate (DSpos10$V_g$bias and DSneg10$V_g$bias); (iii) drain-source in both polarities with an applied bias of -20 V on the gate (DSpos-20$V_g$bias and DSneg-20$V_g$bias). The results of these tests are the object of this section and they will be reported following the same division-criteria as done for P3HT in the previous section. The experimental metrics used to obtain both the TLP parameters and the electrical parameter are the same adopted for the P3HT and in 3.2.2.3 described.

3.2.3.2.1 Positive Drain-source-no gate bias (DSpos)

The DSpos test results fatally damaging to PBTTT OFET devices. The maximum I_{LEAK} registered is 97 μA, by far lower than the I_{FAIL} threshold (0.5 mA) and its shape underlines a progressive loss of the current conductance across the DUT, mostly due to a damage of the interdigitated patterns. The TLP graphs depict one or more clear snapbacks for each of the device tested, confirming that a permanent damaging is occurring (Figure 3-45). I_{LEAK} was found coherent with the I_{TLP} behaviour, suddenly changing in correspondence of the activation of the snapbacks. The TLP parameters are reported in Table 13. There is a channel length influence on the TLP features inasmuch both I_{TR} and V_{TR} follow a trend channel-length dependent, namely with the channel length decreasing the V_{TR} decreases and the I_{TR} increases (Figure 3-46). The R_{TLP} is found ranging between 2.2 kΩ and 0.8 kΩ decreasing as the channel length shortening. A shorter channel yields higher current causing a faster rupture, so explaining the lower R_{TLP}, which is connected to the slope of the I_{TLP} vs V_{TLP} graph.

The DC graphs (Figure 3-47) confirmed that a permanent damage of the devices occurred, featured by a complete loss of the current conductance. Figure 3-48 shows the metal lines of the interdigitated pattern damaged after the TLP tests. No post TLP electrical characterization is performed since no working devices are left.

Table 13: The TLP parameters of the DSpos tested PBTTT OFETs.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.157±0.006	301±4.64	47.2±2.51	4.25±0.23	2.16±0.05
10 µm	0.231±0.004	295±1.63	68.16±1.51	6.13±0.13	1.76±0.26
5 µm	0.29±0.025	271±2.86	78.76±7.73	7.09±0.71	0.92±0.12

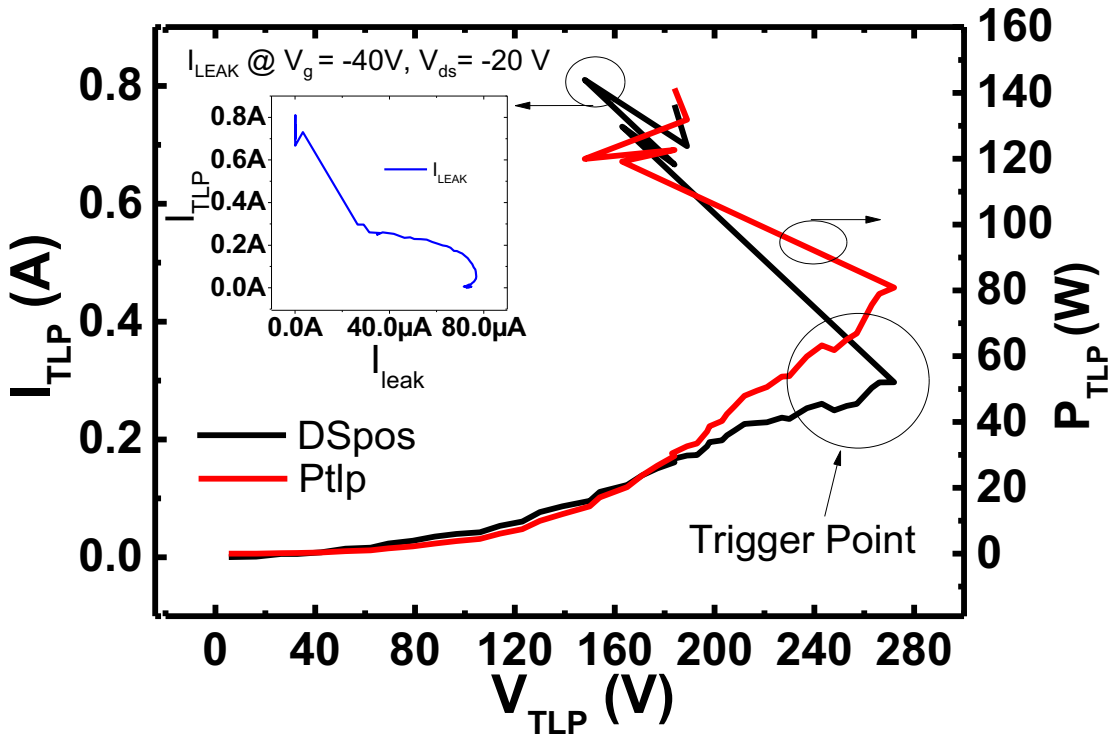


Figure 3-45: The TLP results obtained on a 5 µm channel length PBTTT OFET in drain-source positive pulses with the gate grounded.

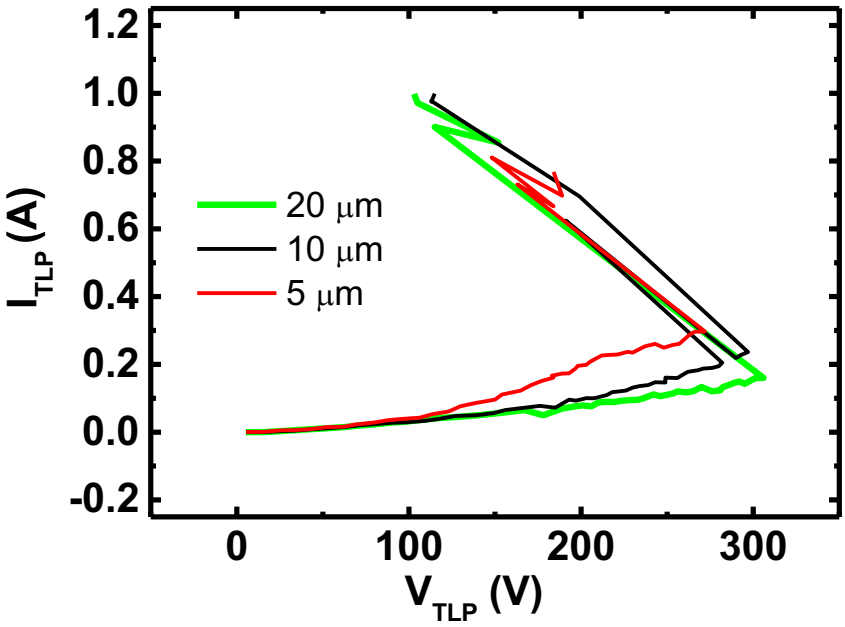


Figure 3-46: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested in the DSpos mode for the PBTTT OFETs. Notably a clear snapback happens in spots linearly increasing in value with the channel length of transistors.

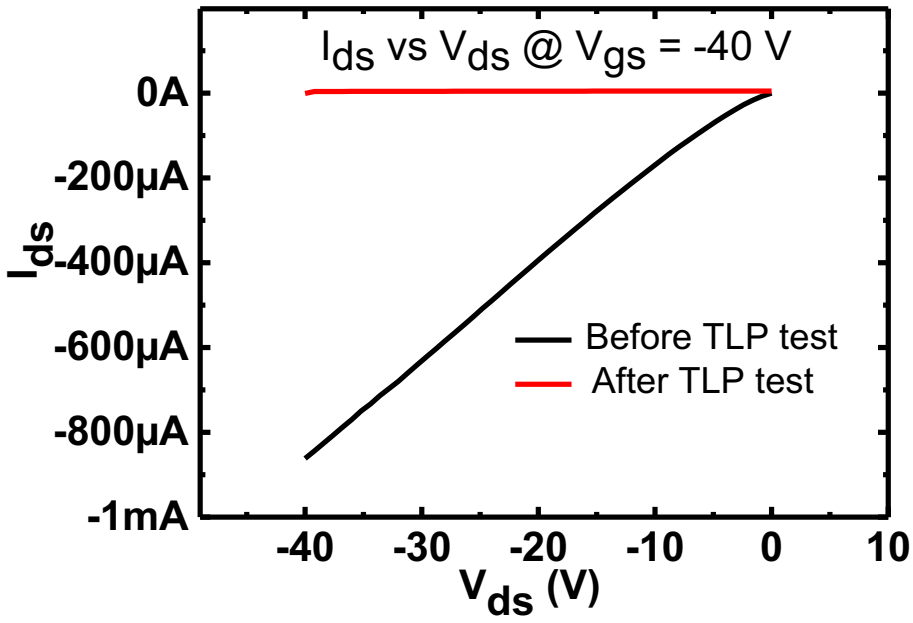


Figure 3-47: The DC behaviour of a 5-μm channel length OFET before and after the positive drain-source TLP test.

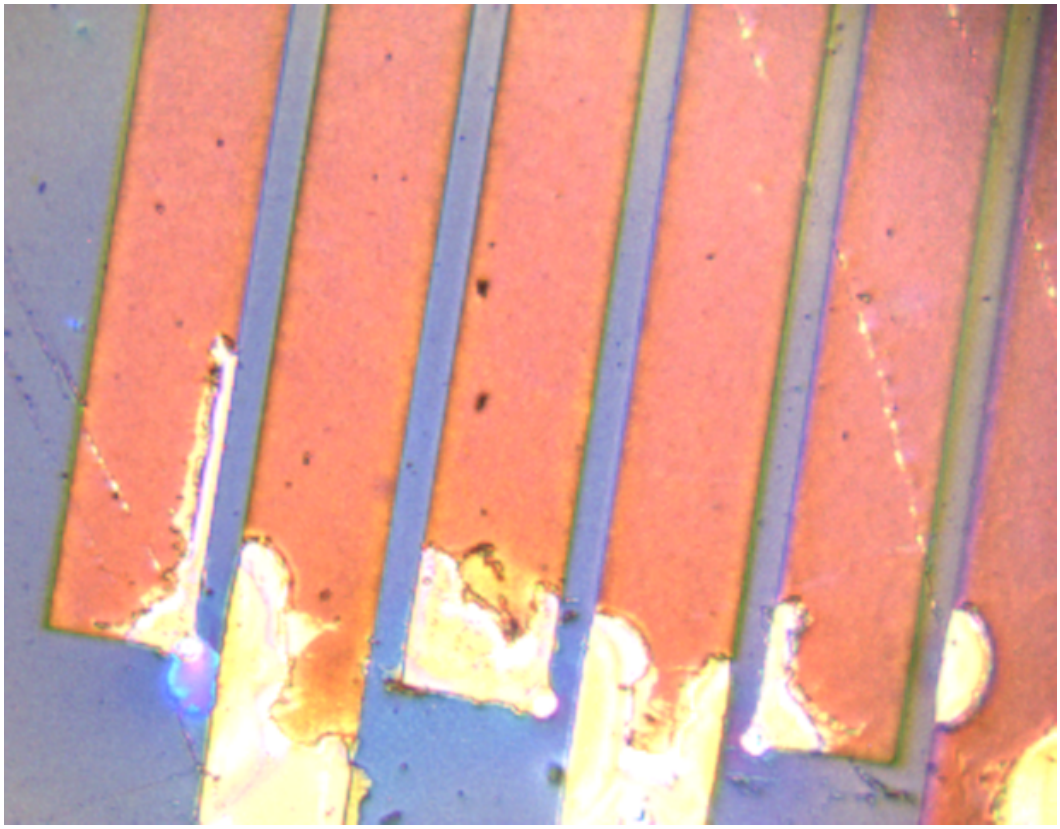


Figure 3-48: The metal lines of a 5-µm channel length PBTT OFET 0 V bias DSPos TLP treated. Damages on the metal lines occurs because of the TLP test. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.3.2.2 Negative Drain-Source-no gate bias (DSNeg)

The DSNeg did not cause any failure to tested devices. The I_{LEAK} resulted lower than 91 µA in all treated devices, pointing out that these devices do not suffer of any arising short circuit. Furthermore, the I_{LEAK} increases linearly with the I_{TLP} up to the first trigger point (Figure 3-49), due to an increase of the DUT conductance probably as a consequence of the polymer heating up, to change immediately afterwards becoming not linear, hence as a sign of a loss of the charge transfer between the TLP system and the DUT. In fact, there is not a clear snapback behaviour, rather several sudden changes of the I_{TLP} values after a first evident change that defines the trigger values. Similarly to what seen in P3HT OFETs tested according DSneg mode, such behaviour is due to a local failure limited to the point of contact between pads and TLP probes. Nevertheless, the TLP parameters were measured and in Table 14 reported. Notably, the maximum pulsed energy is always lower than 2 µJ, as observed in the other cases involving negative pulses between the drain and the source contacts. There is not a linear trend linked to the channel length (Figure 3-50), with the 5 µm-channel length OFETs featuring the lowest value of V_{TR} and the 10 µm ones the highest. The

absence of a trend linked with the geometrical factors of the channel is a consequence of the pulses not involving directly the channel itself. Looking at the DC curves (Figure 3-51) we do not observe any variation of the device behaviour, and pictures of the devices (Figure 3-53) surface do not point out any damage to the device structure. The IV curves and the electrical parameters measured before and after the TLP tests are reported in Figure 3-52 and in Table 15 respectively. The IV curves show a tenfold reduction of the on/off ratio and notably an increase of the V_{TH} up to approximately 10 V.

Table 14: The TLP parameters of DSneg tested PBTTT OFETs.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.04±0.005	219±10.4	8.67±1.5	0.79±0.14	5±0.15
10 µm	0.05±0.004	254±4.1	12.75±1.2	1.16±0.11	5.2±0.05
5 µm	0.03±0.01	110±8.5	2.97±1.4	1.41±0.27	5.8±0.15

Table 15: The electrical parameters of PBTTT OFETs prior and after the DSneg test.

DUT	Mobility ($x10^{-2}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^3$)
Pristine	6.04±1.42	-9.06±2.2	5.3±0.6
Post DSneg test	2.69±3.4	10.09±1.3	0.4±0.05

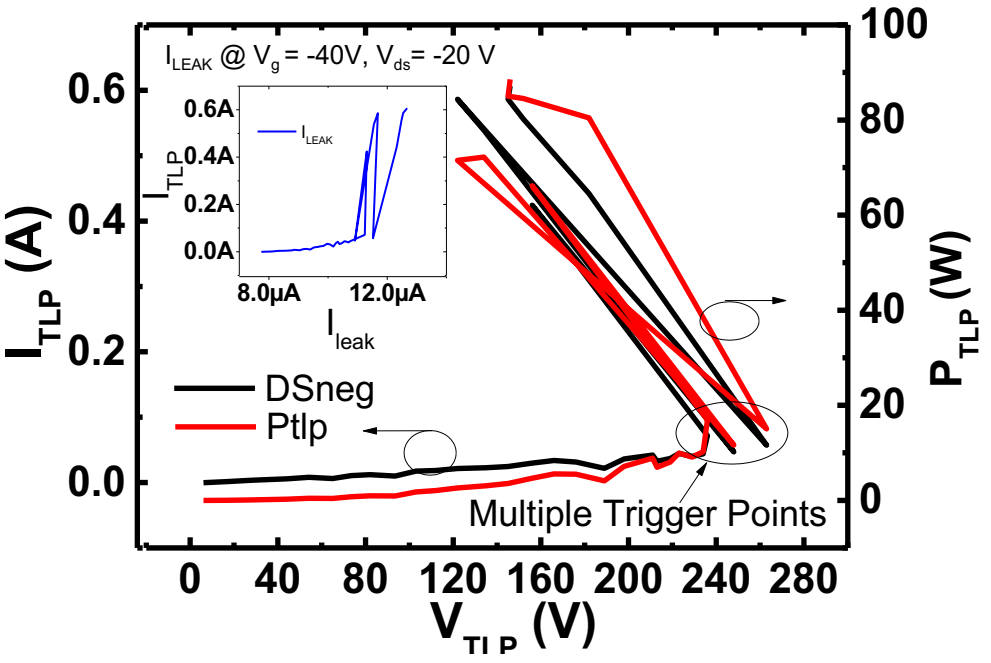


Figure 3-49: The TLP results obtained on a 20 μm channel length PBTTT OFET in drain-source negative pulses no bias modality.

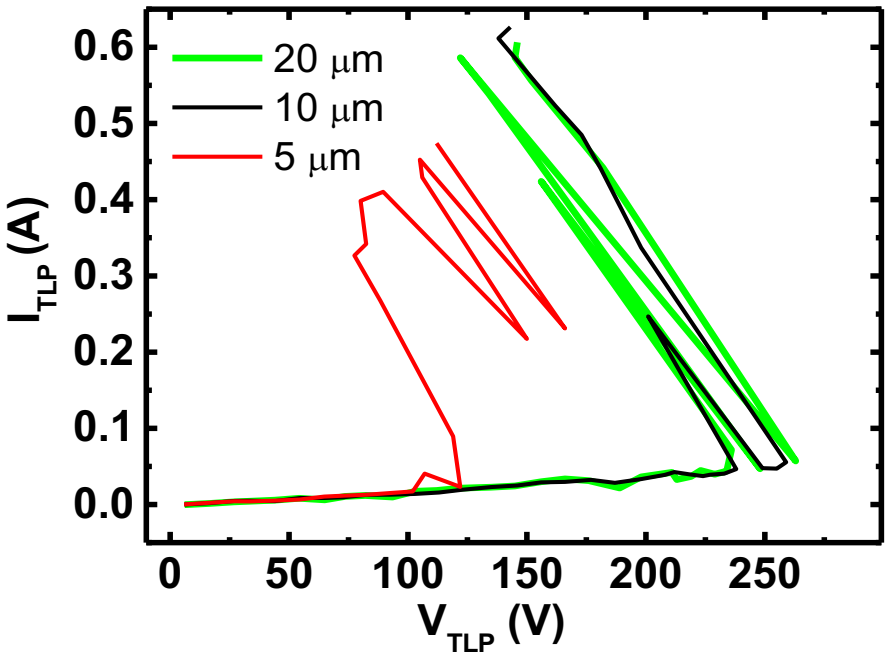


Figure 3-50: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested. There is a marked difference between the 5 μm-channel length and the other cases, in which instead the differences are feeble.

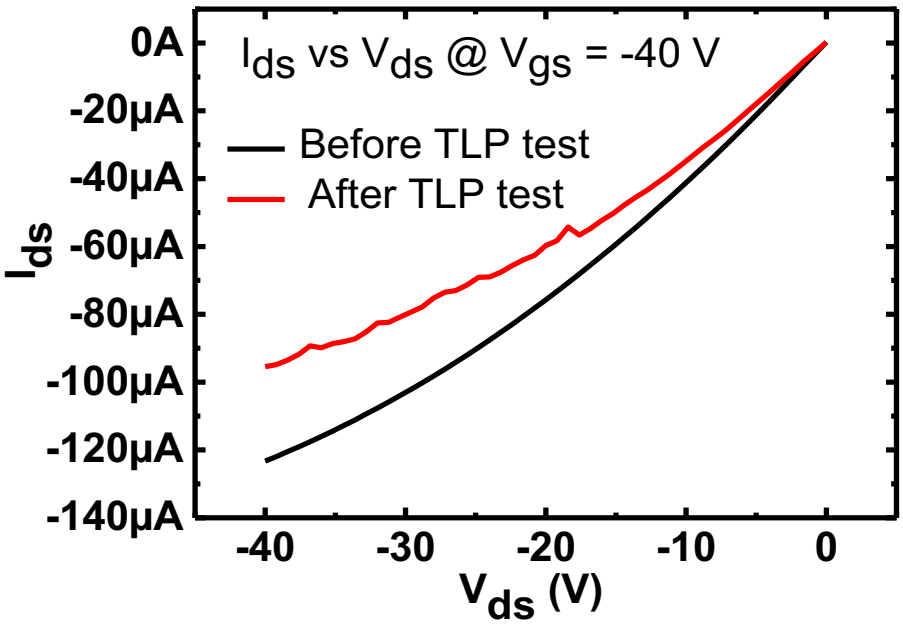


Figure 3-51: The DC behaviour of 20-µm channel length OFET before and after the negative drain-source TLP test. The device keeps his functionality but the shape of the curve is slightly altered.

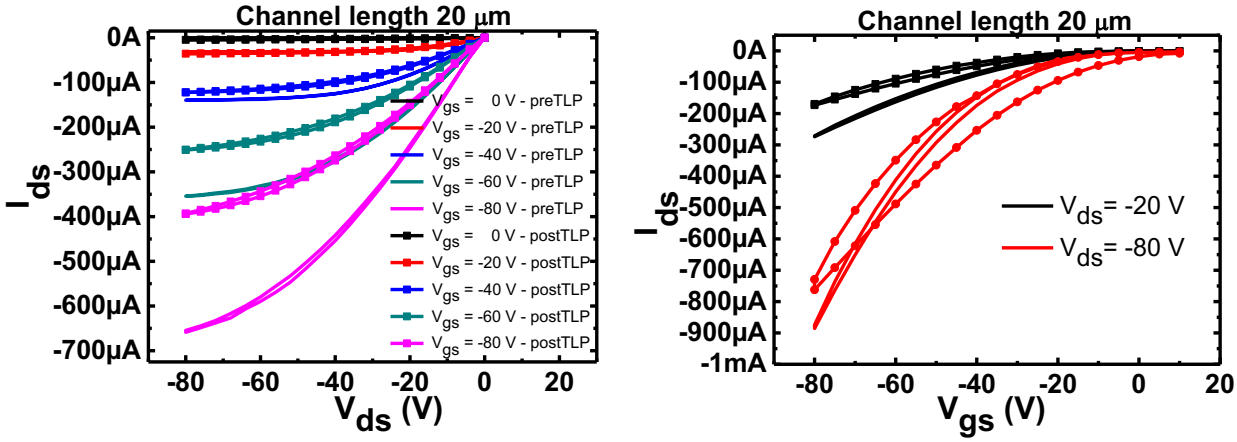


Figure 3-52: the IV curves of a 20µm channel length PBTTT OFET before and after the DSneg test.

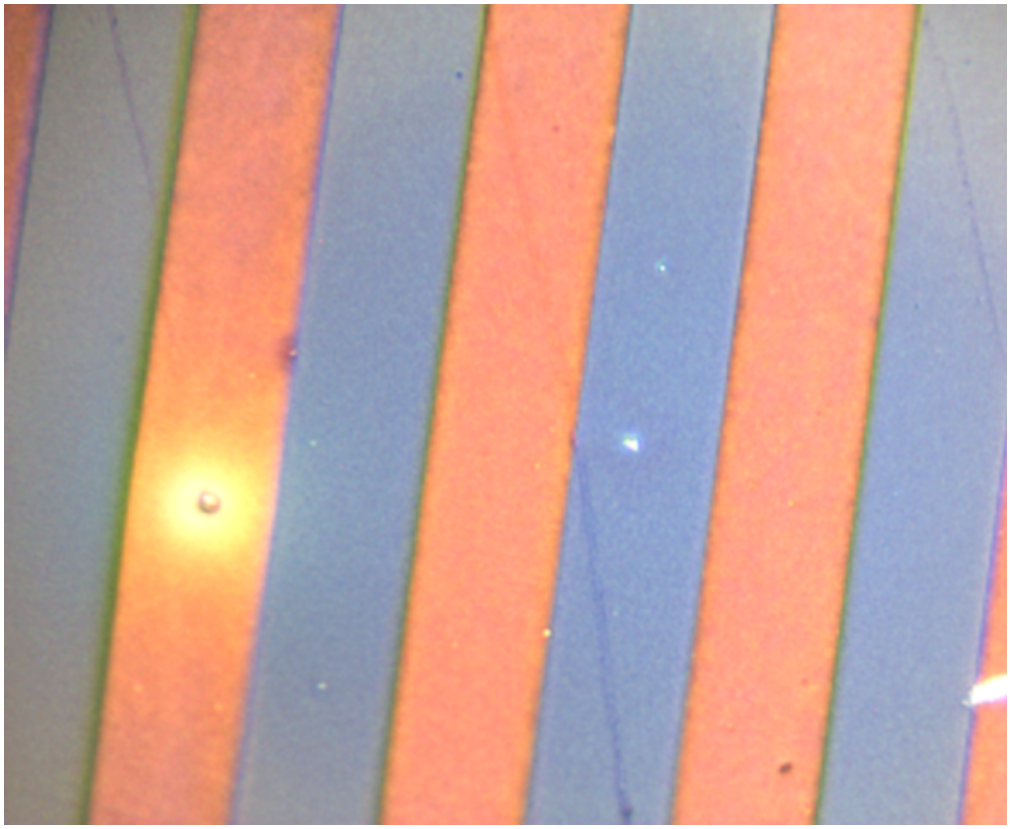


Figure 3-53: The top view of a 20µm channel length PBTTT OFET device. No major damages over the metal lines are visible. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.3.2.3 Positive Drain-source-V_g bias 10 V (DSpos10$V_g$bias)

All the OFETs tested according to the DSpos10$V_g$bias test suffered a failure. The I_{LEAK} was found lower than 194 µA in all cases, hence no short circuits arise because of the test. The TLP parameters were calculated and in Table 16 reported. The pulse mean duration is 92 ns. There is a channel length linear dependence of such parameters with the decreasing of the channel length (Figure 3-55), as expected, being the channel directly interested by the pulses. The I_{TLP} vs V_{TLP} graphs point out a clear snapback in all cases (Figure 3-54), therefore indicating a spoiling of the devices, corroborated by the I_{LEAK} that is progressively reduced during the TLP test before the trigger point and no longer following linearly the I_{TLP} afterwards. The joint effect of the clear snapback and of the I_{LEAK} reduction are clearly due to a permanent damage of the devices. The DC test (Figure 3-56) confirms a deterioration of the devices. Pictures of the devices (Figure 3-57) reveal that the metal lines were destroyed. I did not carry out any post TLP electrical analysis since no working devices were left.

Table 16: The TLP parameters of DSpos10V$_g$bias tested devices.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.17±0.006	297±1.6	51.04±2.06	4.65±0.19	1.8±0.04
10 µm	0.22±0.012	285±6.4	65±4.81	5.91±0.44	1.7±0.02
5 µm	0.21±0.02	210±10.5	45.21±6.74	4.11±0.61	1.2±0.13

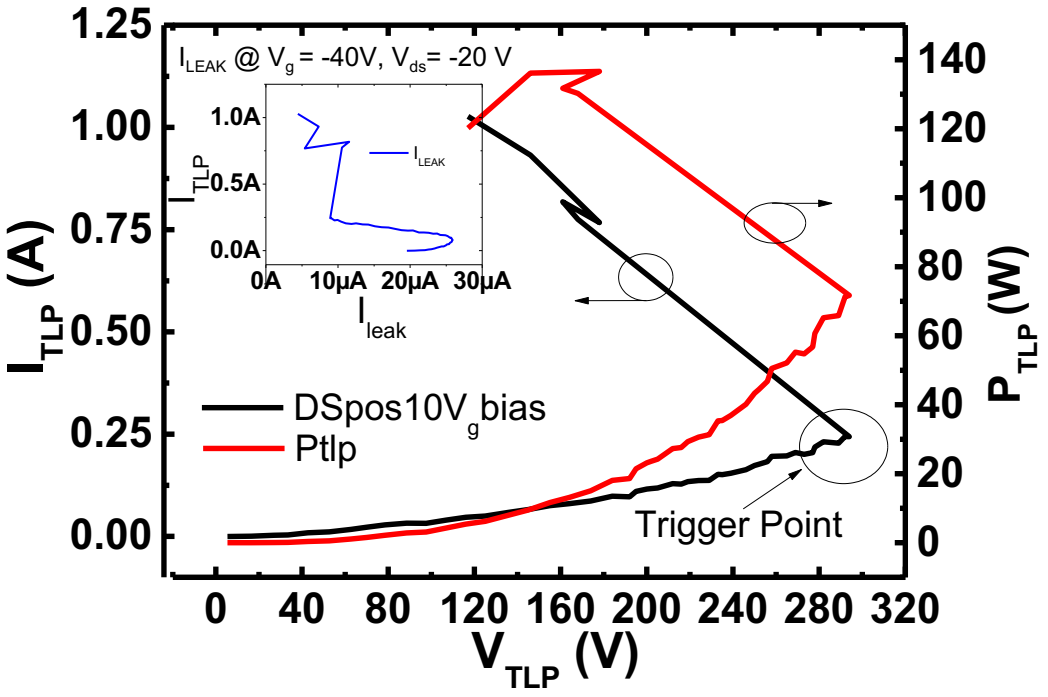


Figure 3-54: The TLP results obtained on a 10 µm channel length PBTTT OFET in drain-source positive pulses 10 V gate-bias modality.

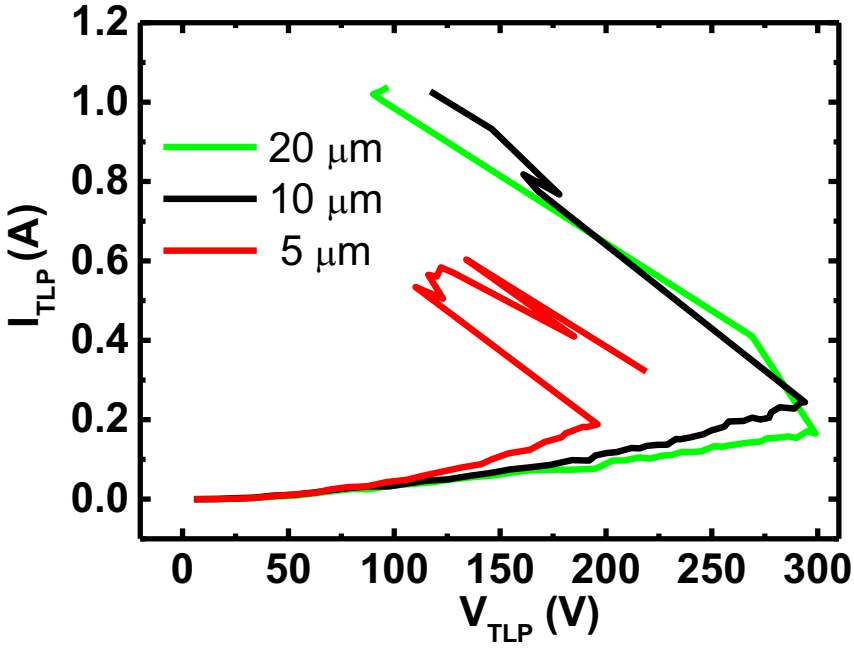


Figure 3-55: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested. A trend depending on the channel lengths can be observed.

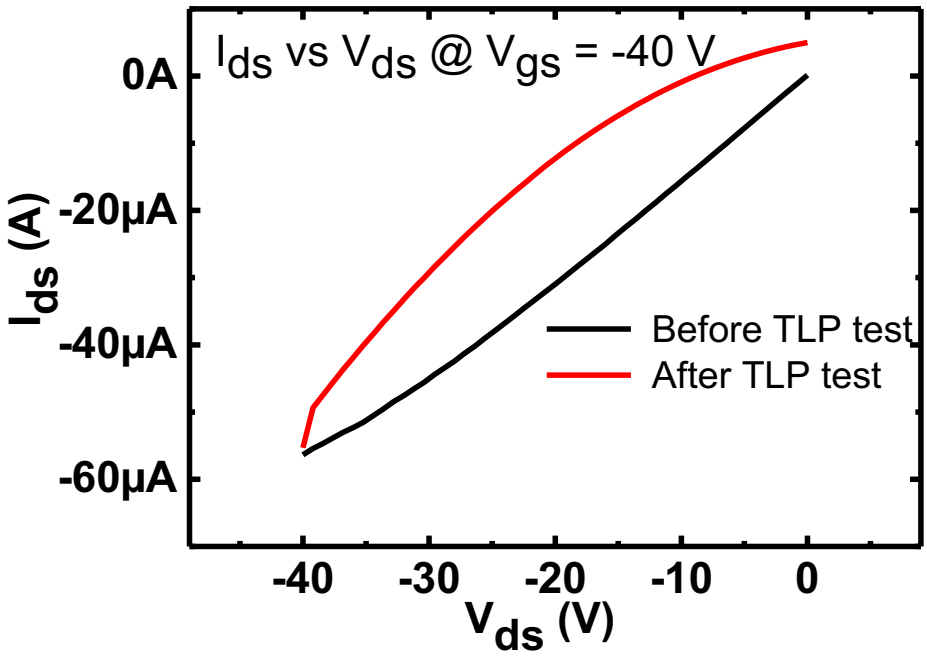


Figure 3-56: The DC behaviour of 10-μm channel length OFET before and after the positive drain-source 10 V gate bias TLP test.

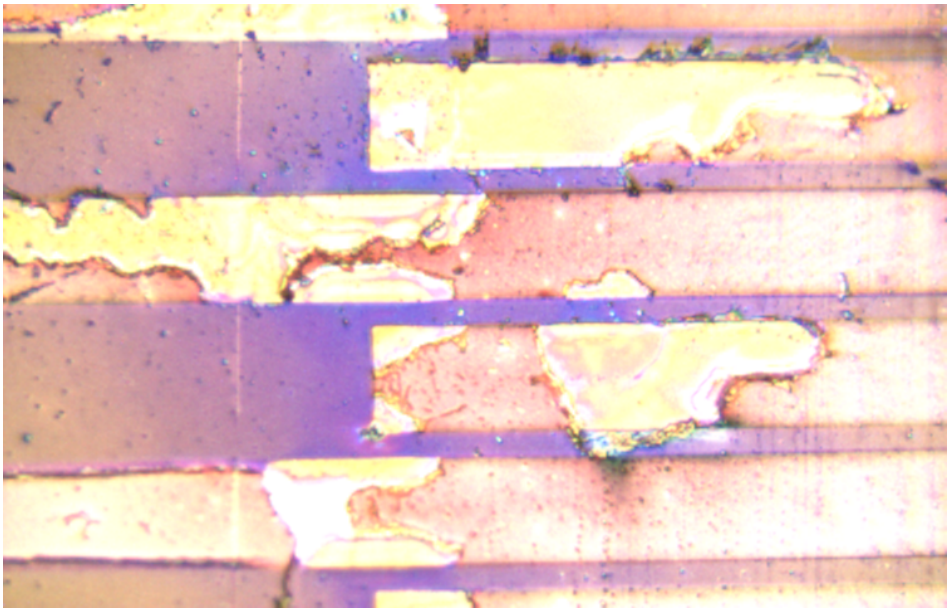


Figure 3-57: The top view of a 10 µm PBTTT device. Heavy damages can be observed. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.3.2.4 Negative Drain-source-Vg bias 10 V (DSneg10$V_g$bias)

Interestingly, the DSNeg10V gate bias test caused a total failure in the 10 µm channel-length devices, whilst the remaining OFETs, although did not lose their electrical capabilities completely, resulted heavily weakened and no longer sufficiently performing. A possible explanation for such response of PBTTT OFETs to the DSneg10$V_g$bias test lies in the devices channel partially opened, since these are forced to work as n-FETs in a forward configuration. Differently to what observed in the other cases involving negative discharges between the drain and the source, a partial transfer of the charges across the devices takes place so overheating the metal lines. The I_{LEAK} in the 10 µm channel-length devices reached a value of 2 mA, hence they exceeded the I_{FAIL} value and reached the set compliance value. Although such value was reached, the I_{LEAK} does not show a short circuit behaviour since it starts decreasing immediately after. Such behaviour is due to the failure of the pad-interdigitated pattern electric contact. In the other cases, the I_{LEAK} was lower than 188 µA and linearly following the I_{TLP} up to the trigger point to decrease afterwards. The TLP parameters are characterised by a great measurement uncertainty (Table 17), hence there is no such a thing as a channel length effect in this case (Figure 3-59). The pulse mean duration is 91 ns. The I_{TLP} vs V_{TLP} graphs show different behaviours between the 10 µm channel-length devices and the others. The latter feature a clear snapback followed by more ones with the I_{LEAK} tendentiously following linearly the I_{TLP} up to the trigger point, and progressively decreasing afterwards, suggesting local ruptures

taking place over the pads so compromising the electric contact between the TLP probe and the OFET. The behaviour of totally failed devices is different suggesting a more complicated interaction between the devices and the discharges (Figure 3-58). The DC tests show a degradation of the device in partially damaged OFETs (Figure 3-60), whereas in those damaged there is a complete loss of every response from the device. The latter behaviour is due to a total destruction of the metal lines. In Figure 3-61, the metal lines of the 10 µm channel length are shown. These feature completely damaged spots, whilst in the 5 µm ones damages are also evident but not impeding the current to flow through. However, the degradation degree is such to render post TLP electrical characterisation futile.

Table 17: The TLP parameters of the DSneg10$V_g$bias tested devices.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.25±0.21	184±34	46.41±54.1	4.22±4.9	4±0.2
10 µm	0.57±0.37	154.7±18	88±74.5	8.01±6.8	2.6±0.3
5 µm	0.19±0.19	186±37	35.13±50.4	3.2±4.6	3.8±0.3

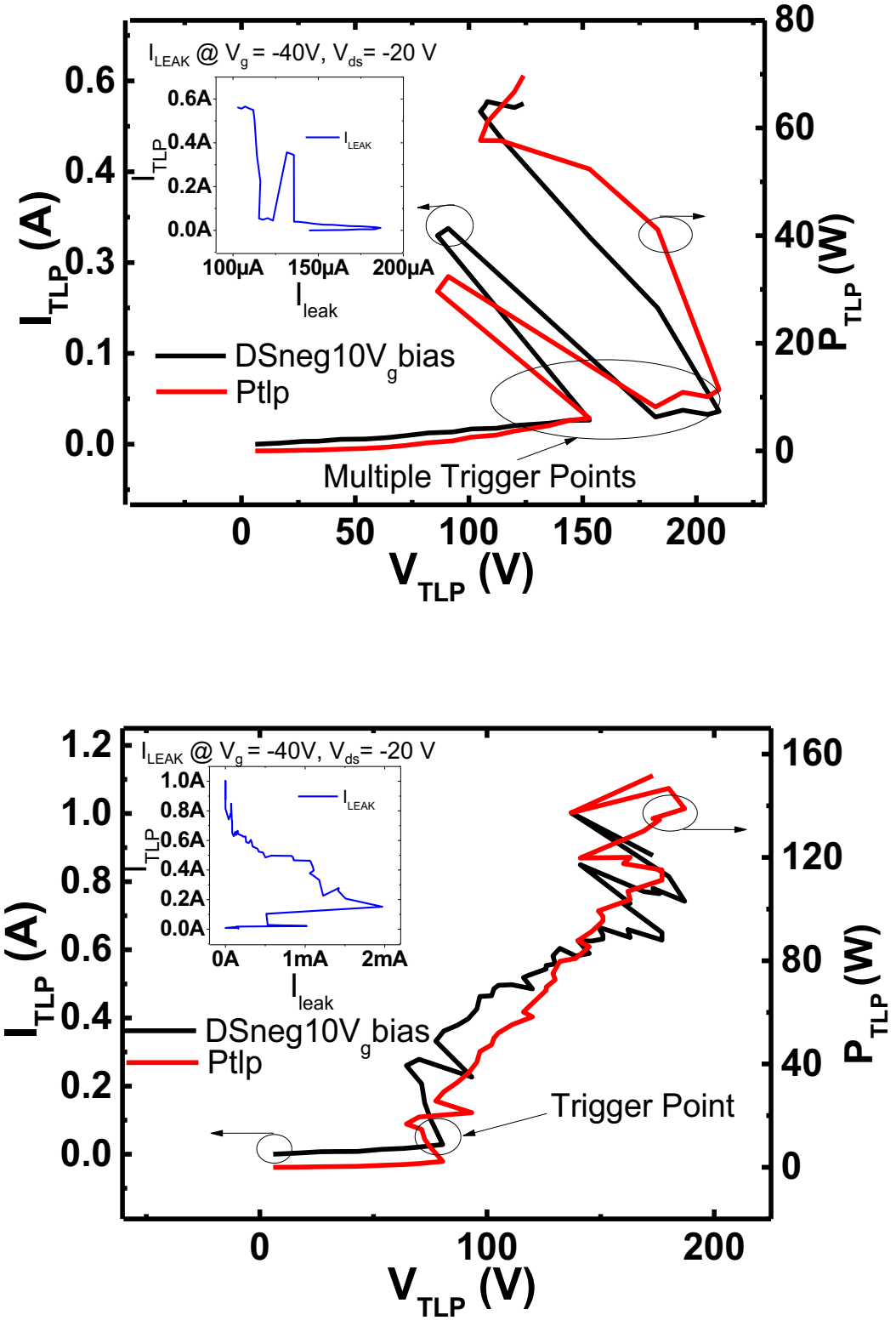


Figure 3-58: The TLP results obtained on a 5 µm channel length (above) and on a 10 µm channel length (below) PBTTT OFET in drain-source negative pulses 10 V gate bias modality.

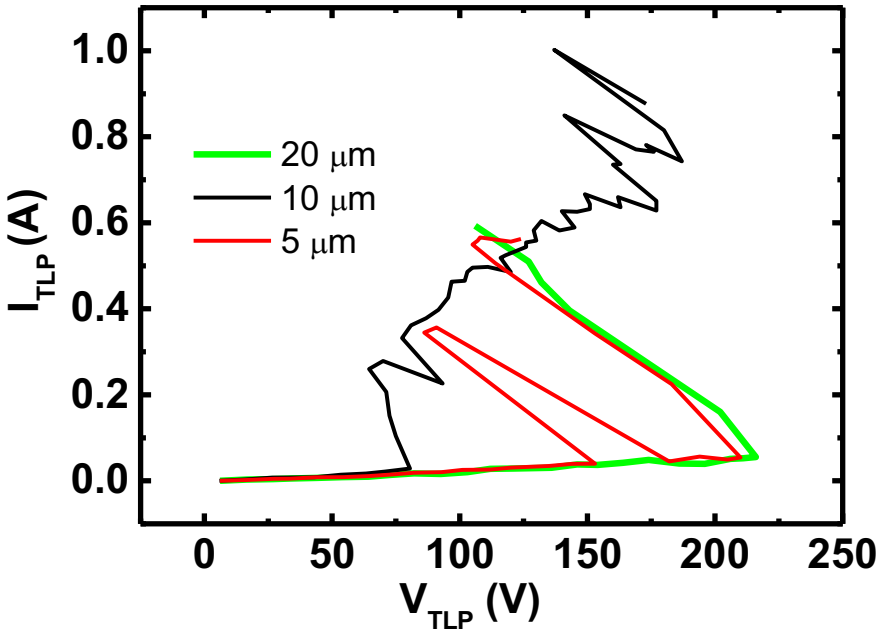


Figure 3-59: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested, revealing how there is no a trend of the features with the change of the channel length.

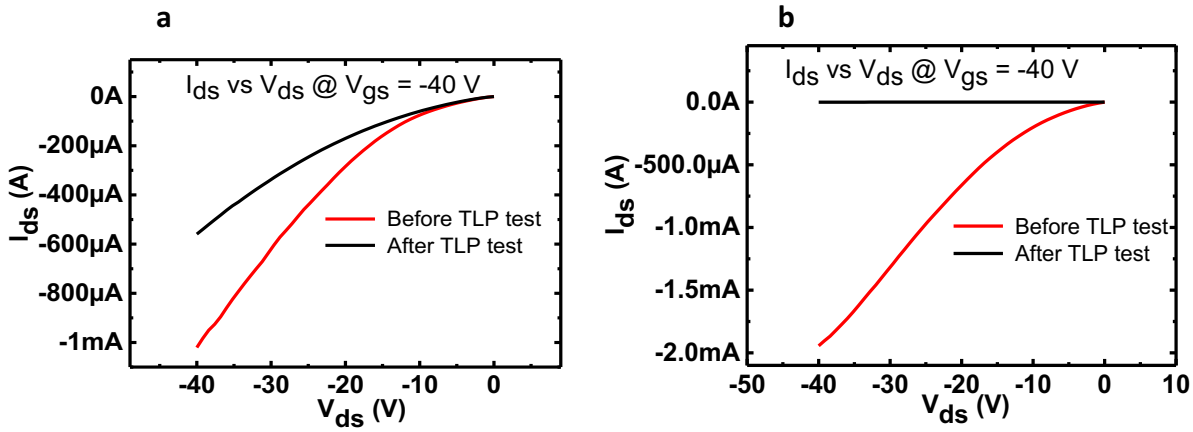


Figure 3-60: The DC results obtained on a 5 μm channel length (a) and on a 10 μm channel length (b) PBTTT OFETs in drain-source negative pulses 10 V gate bias modality.

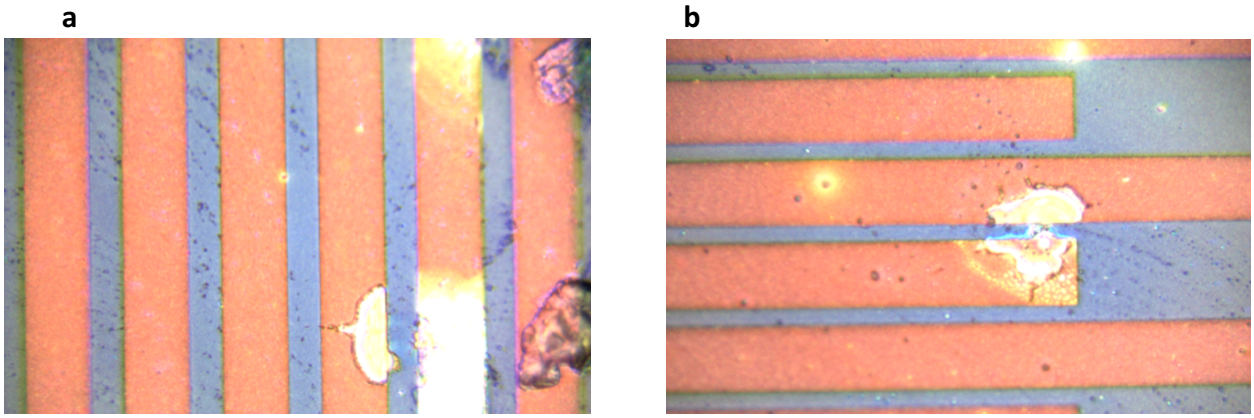


Figure 3-61: The top view of a 10 µm (a) PBTTT device and of a 5 µm device (b). Heavy damages with a loss of electric conduction is visible in the left image, whilst partial damages are visible on the right. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.3.2.5 Positive Drain-source-Vg bias -20 (DSpos-20$V_g$bias)

The DSpos-20$V_g$bias test induces a total failure in only one of the tested devices (a 10 µm-channel length). However, a significant degradation was observed in the rest of the samples tested. The response to the pulsed energy of the PBTTT is hence different to what observed in the case of P3HT OFETs tested in this same modality. In fact, the latter destroyed all the tested devices. An explanation to such behaviour lies in the PBTTT higher charge mobility than the one featured by P3HT, therefore resulting into a higher reactivity with respect to the pulsed charges that are more efficiently transported and dissipated through the device itself, and only partially dissipated over the device metal lines via ohmic heating. In fact, in this modality the FETs channel is opened and the charges are allowed to flow through. The pulse mean duration is 90 ns. The I_{TLP} vs V_{TLP} graphs show a clear snapback in all cases analysed (Figure 3-62). In the device that did not suffer a total failure the I_{LEAK} is always lower than 121 µA, whereas it exceeds the I_{FAIL} value in the destroyed one reaching a value of approximately 1 mA. In all cases analysed, the I_{LEAK} increases up to the point in which the I_{TLP} reaches the trigger value to dramatically decrease afterwards, so releasing the pulsed energy via parasitic electric paths forming through the device. Notably, none of the transistors resulted short-circuited. The TLP parameters were calculated and in Table 18 are reported. There is a feeble channel length dependence of such parameters with the decreasing of the channel length (Figure 3-63). The DC tests (Figure 3-64) confirmed the failure of one of the devices whilst a kept functionality in the others. Therefore, the devices withstanding the TLP test eventually resulted only reduced in their electrical features. Pictures (Figure 3-66) of the devices do not show superficial damages, except in the broken one that appears burnt in some spots over the metal lines. The IV curves and the electrical parameter of the PBTTT OFETs measured before and after the

DSpos-20$V_g$bias test in Figure 3-65 and in Table 19 are respectively reported. There is a tenfold reduction of the on/off ratio affecting the tested devices whilst the V_{TH} and the mobility are reduced in the mean value.

Table 18: The TLP parameters of the DSpos-20$V_g$bias tested devices.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.16±0.01	276±12	45.92±5.16	4.13±0.5	1.9±0.06
10 µm	0.19±0.03	259±10	51.78±9.78	4.66±0.8	1.3±0.09
5 µm	0.24±0.14	240±8	57.57±5.45	5.18±0.5	0.8±0.06

Table 19: The electrical features of PBTTT OFETs before and after the DSpos-20$V_g$bias test.

DUT	Mobility ($x10^{-2}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^3$)
Pristine	3.94±0.3	-9.22±2.7	2.4±0.2
Post DSpos-20$V_g$bias test	2.87±3.3	-2.87±3.3	0.18±0.2

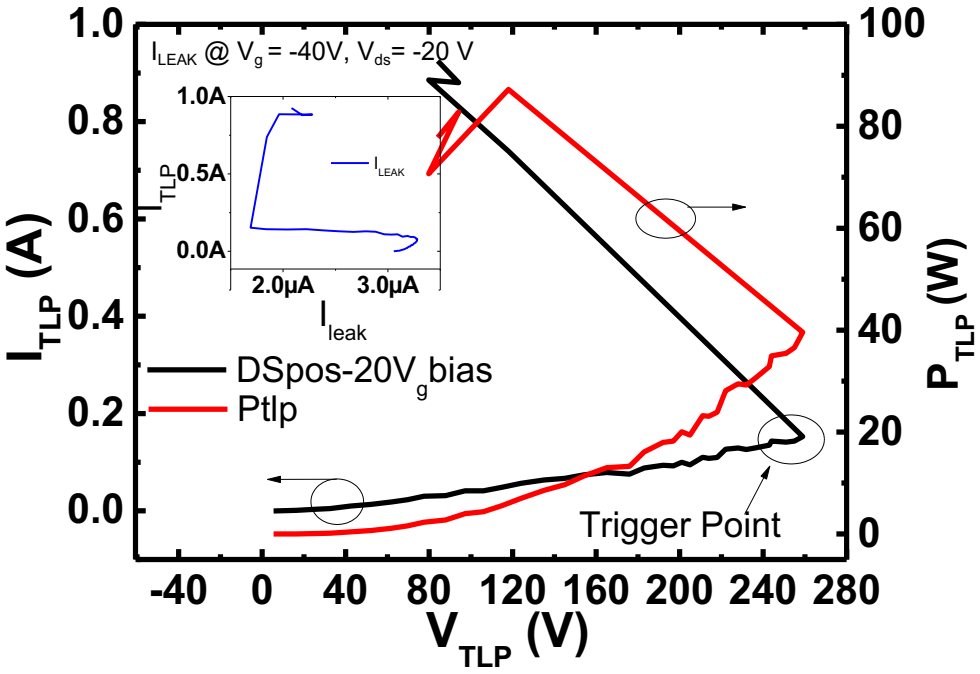


Figure 3-62: The TLP results obtained on a 20 μm channel length PBTTT OFETs in drain-source positive pulses with -20 V gate bias.

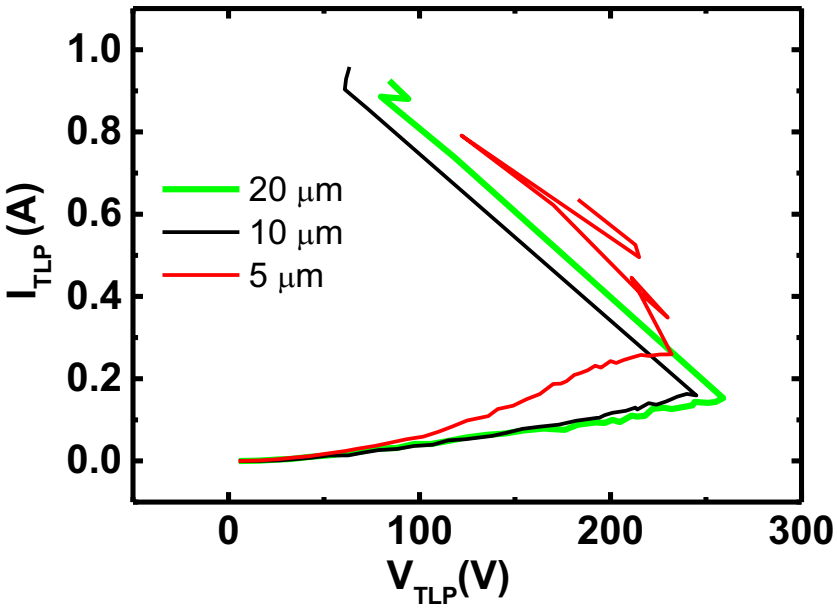


Figure 3-63: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested revealing, although feeble, a trend of the features with the change of the channel length.

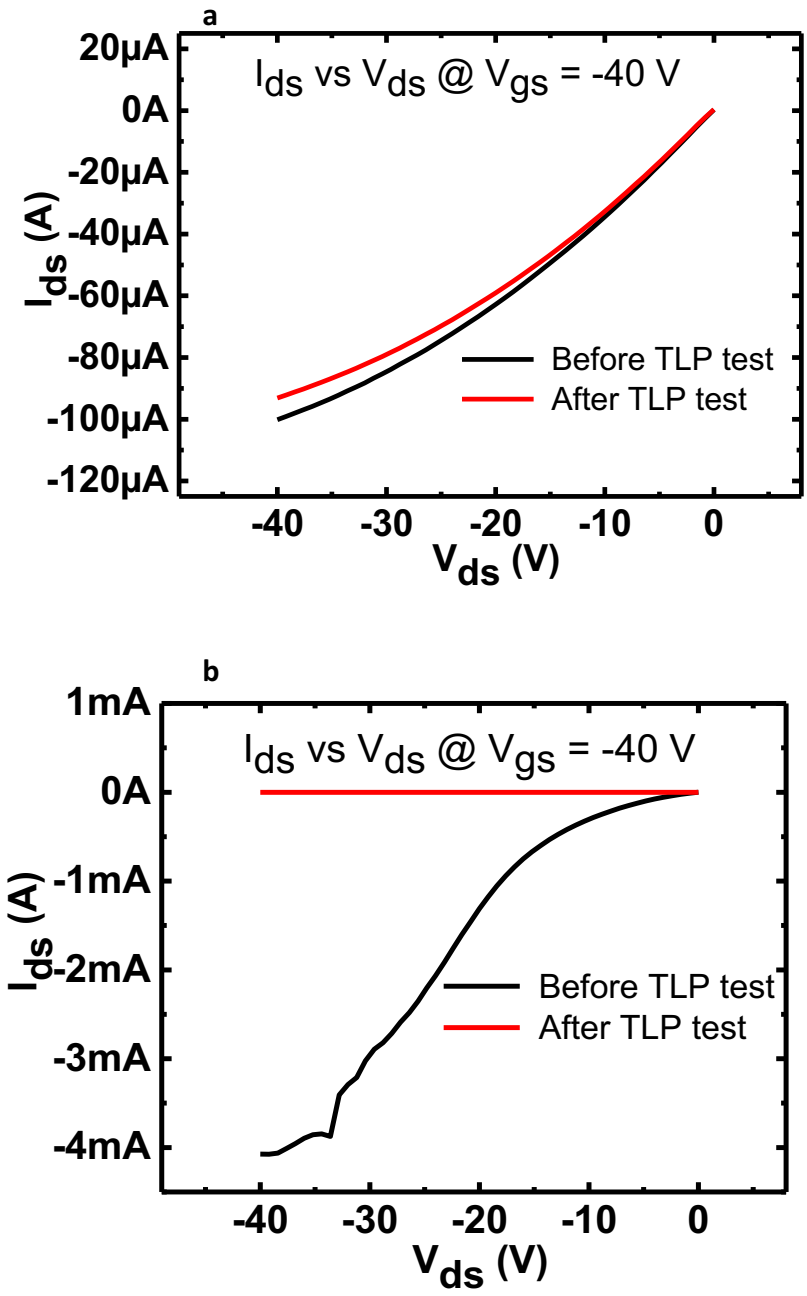


Figure 3-64: The DC results obtained on a 10 μm channel length (a) and on a PBTTT OFETs in drain-source positive pulses with -20 V gate bias.

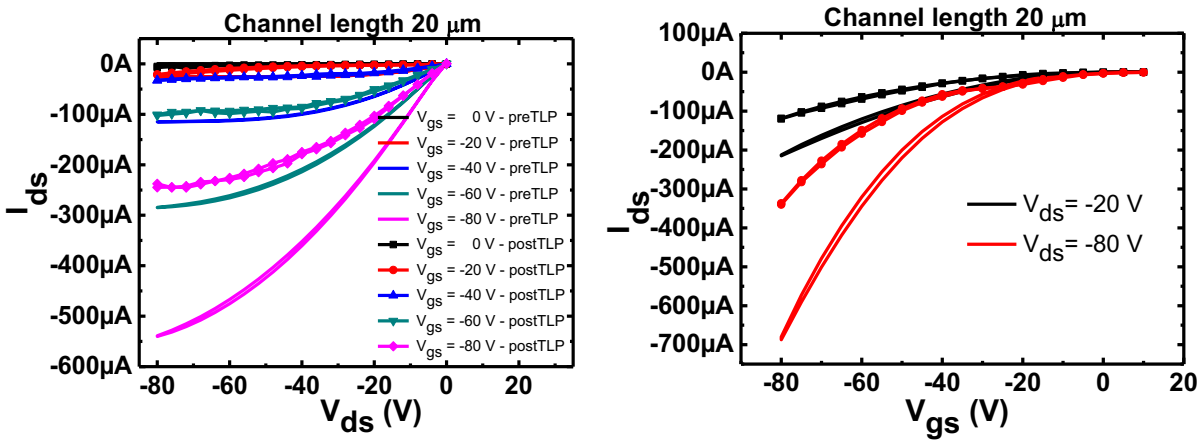


Figure 3-65: The IV curves of a 20 µm-channel length PBTTT OFET measured before and after being tested according to the DSpos-20V$_g$bias mode.

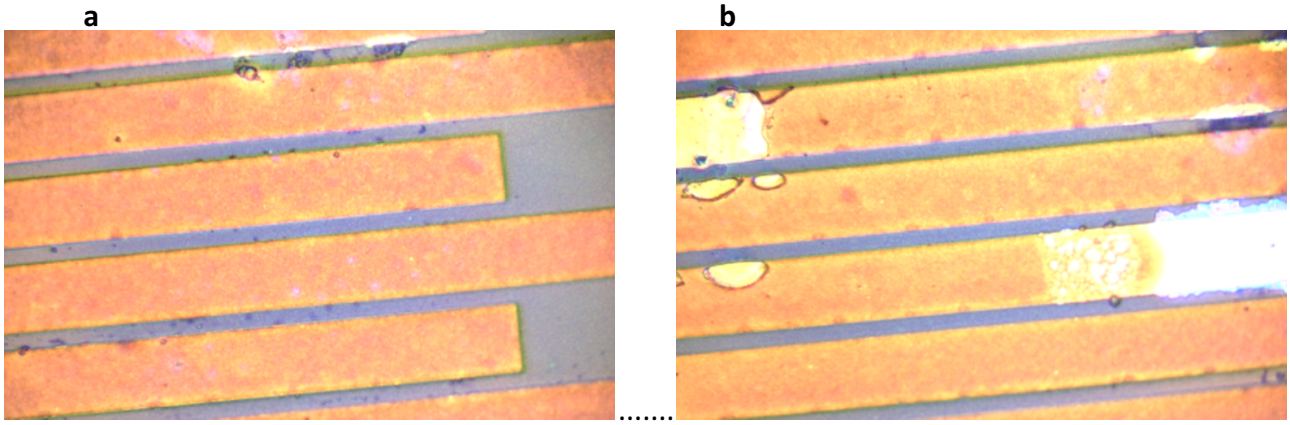


Figure 3-66: The top view of a 5 µm PBTTT device tested according to the DSpos-20V$_g$bias test that reported only minor damages (a) and of the device of the same kind tested in the same TLP conditions that instead reported major damages (b). Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.3.2.6 Negative Drain-source-Vg bias -20V (DSneg-20V$_g$bias)

The DSneg-20V$_g$bias test did not cause the failure of the tested devices. An explanation to this behaviour lies into the pulsed energy not finding a chance to flow through the devices since the polarisation of the device is opposite to the pulsed charges and therefore creating a barrier that stops charges locally so preventing a fatal heating of the internal interdigitated patterns. Such response causes the local rupture of the TLP probe-pad electrical contact, similarly to what observed in the DSneg test of PBTTT OFETs and the tests involving negative pulses between drain and source in P3HT OFETs. The flow of the electric charges from the TLP probe to the device under test results interrupted because of such failure. The I_{LEAK} was found always lower than 61 µA, hence none of the

Table 20: The TLP parameters of the DSneg-20V$_g$bias tested PBTTT OFETs.

	I_{TR} (A)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
20 µm	0.07±0.002	256.6±4.7	19.22±0.9	1.77±0.08	3.9±0.08
10 µm	0.064±0.003	247±10.2	15.86±1.5	1.46±0.14	3.9±0.14
5 µm	0.07±0.005	254.3±3.1	17.85±1.4	1.64±0.13	4±0.06

devices failed the I_{LEAK} test. The TLP parameters were calculated and in Table 20 reported, the pulse mean duration is 92 ns. There is not a channel length effect in this case since the pulses did not involve directly the channel itself (Figure 3-68). The I_{LEAK} remains stuck to a certain value straight after the I_{TRIG}, not following the increasing I_{TLP}. The I_{TLP} vs V_{TLP} graphs show a first clear trigger point followed by other ones, confirming a local arising discontinuity in the electric path between the pad and the TLP probe (Figure 3-67). This, as seen before, prevent the devices to incur to a systemic failure, as confirmed by the DC graphs (Figure 3-69) and the pictures of the tested devices (Figure 3-71), which do not point out superficial damages. As showed in the IV curves measured before and after the test in Figure 3-70, despite the devices did not suffered a failure, these eventually resulted strongly weakened by the test so that I did not carry out any post TLP electrical parameters analysis.

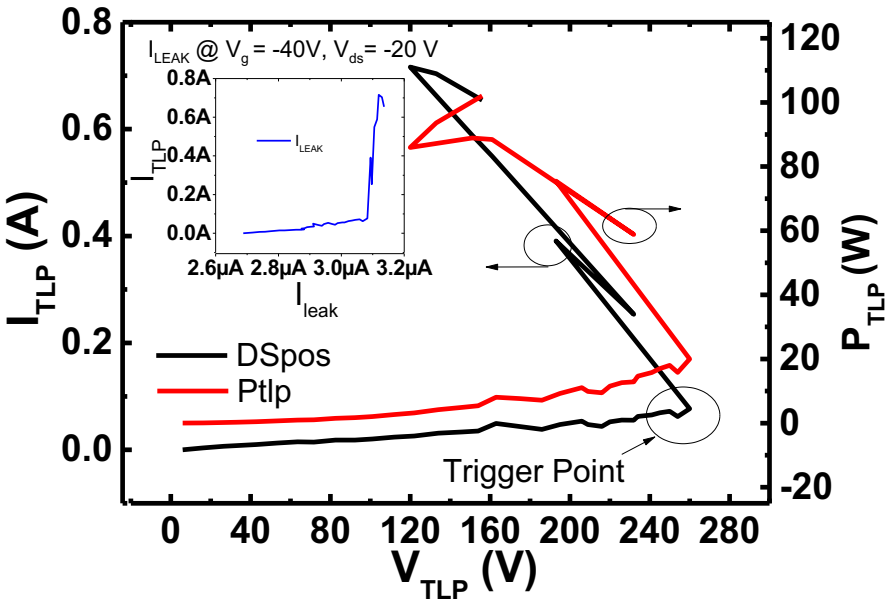


Figure 3-67: The TLP results obtained on a 20 µm channel length PBTTT OFETs in drain-source negative pulses -20 V gate bias modality.

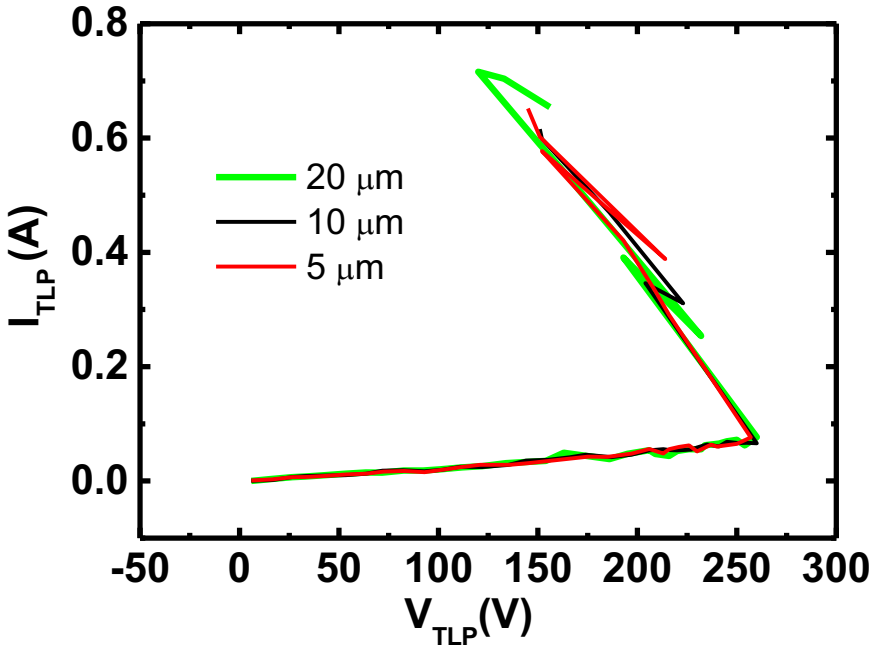


Figure 3-68: The TLP I_{TLP} vs V_{TLP} graphs for all the channel lengths tested, revealing there is not a trend of the features with the change of the channel length.

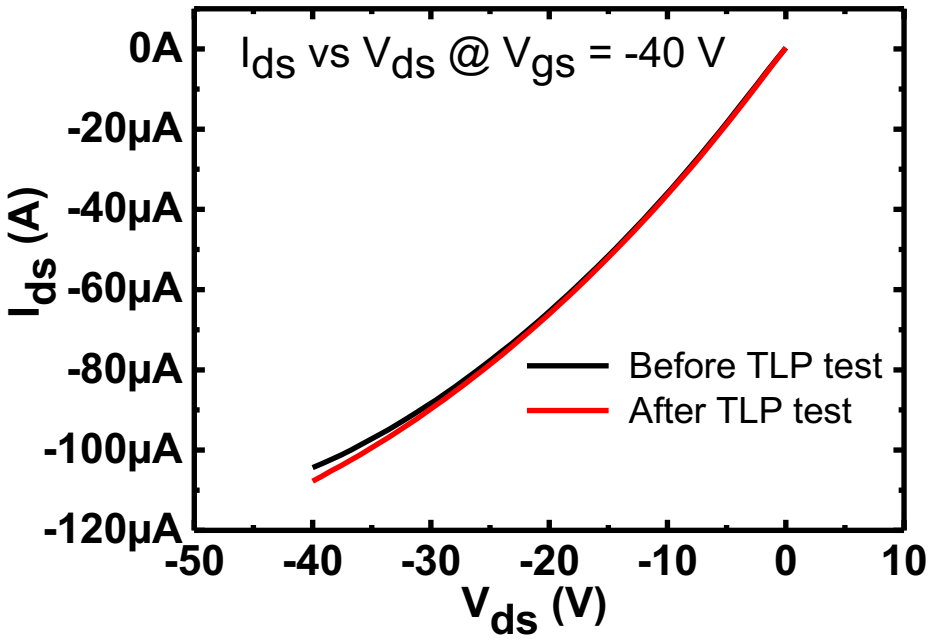


Figure 3-69: The DC results obtained on a 20 μm channel length PBTTT OFETs in drain-source negative pulses - 20 V gate bias modality.

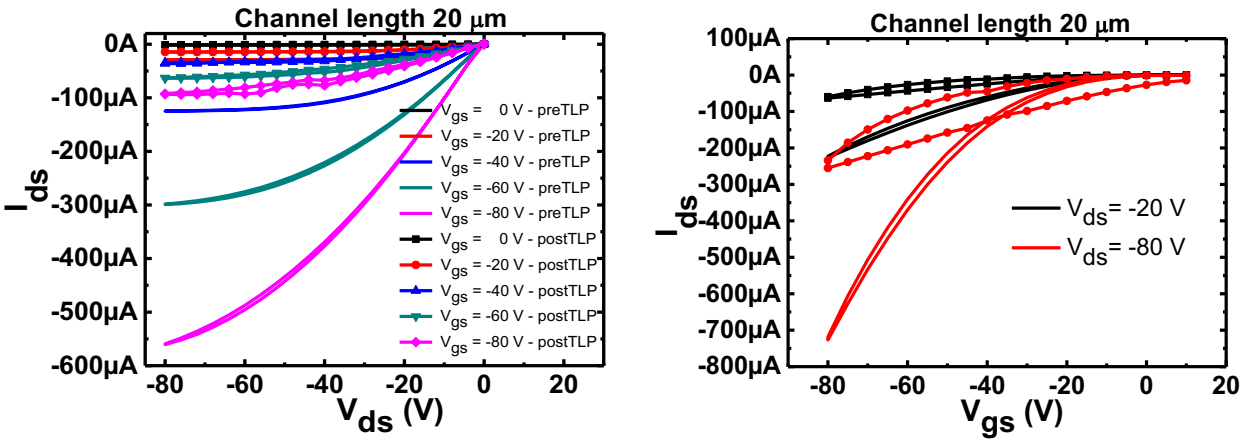


Figure 3-70: The IV curves of a 20 µm-channel length PBTTT OFET measured before and after the DSneg-20V$_g$bias mode.

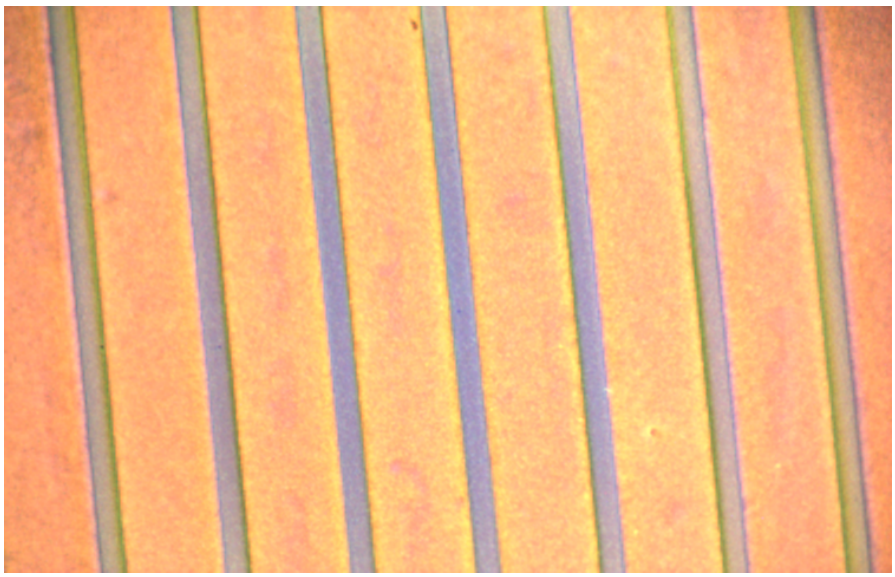


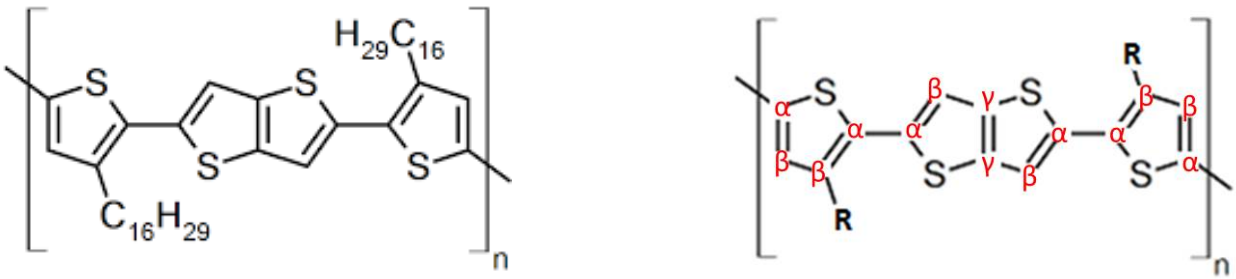
Figure 3-71: The top view of a 10 µm PBTTT device. No evident damages are visible in the image. Images were taken by means of a USB camera embedded within the Renishaw InVia Microscope, 50x zoom.

3.2.3.3 *Raman spectra of the TLP tested PBTTT OFETs*

The Raman spectra were collected from each of the tested devices and compared with reference spectra taken from a pristine device, namely built within the same fabrication session of the other ones and according to the same procedure and by using the very same materials, by focusing the laser beam over an area located in the middle of two metal lines of the interdigitated pattern of a 5 µm channel length. The Raman spectra reported were obtained by normalising each spectrum to

the 1391 cm^{-1} thiophene C-C stretch mode peak (C_β-C_β intra-ring stretching) generated in the PBTTT spectra.

A representative spectrum per each TLP case was chosen and in Figure 3-73 reported. Such graph is then split in two other graphs, in the first one the portion 1250 to 1550 cm^{-1} of the original spectra is analysed (Figure 3-74 above) whilst the portion 600 to 1250 cm^{-1} is analysed in the second one (Figure 3-74 below). The mechanical vibrations of the molecular bonding are described also referring to the α- and β- positions[10] of carbons within the thiophene and the thienothiophene rings composing the polymer (Figure 3-72).



.....

Figure 3-72: PBTTT molecular structure (left) and carbon positions within the thiophene and the thienothiophene rings (right).

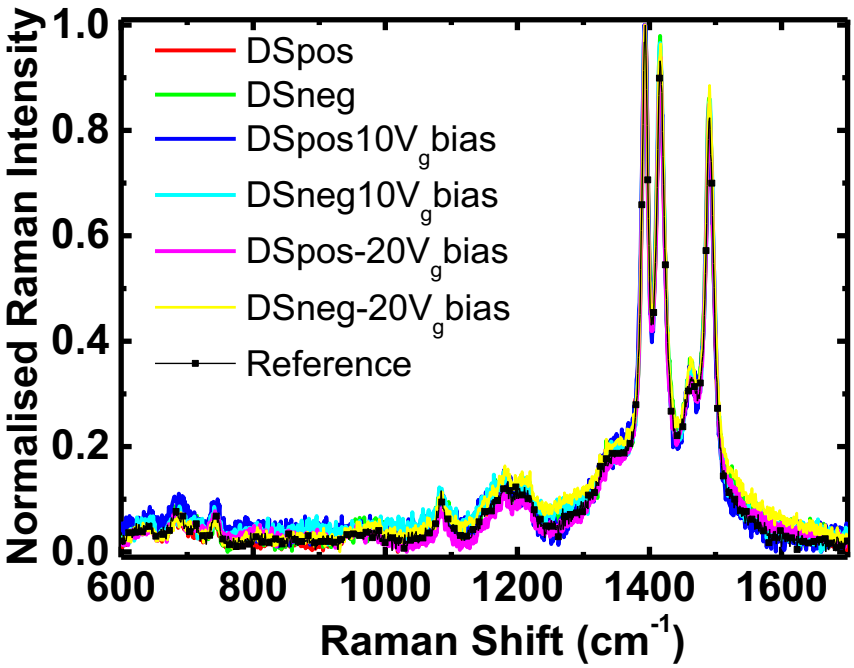


Figure 3-73: The normalised Raman spectra, within the range 600-1650 cm^{-1}, of the PBTTT OFETs. Spectra were collected from all the TLP-tested devices and compared to those collected from pristine ones.

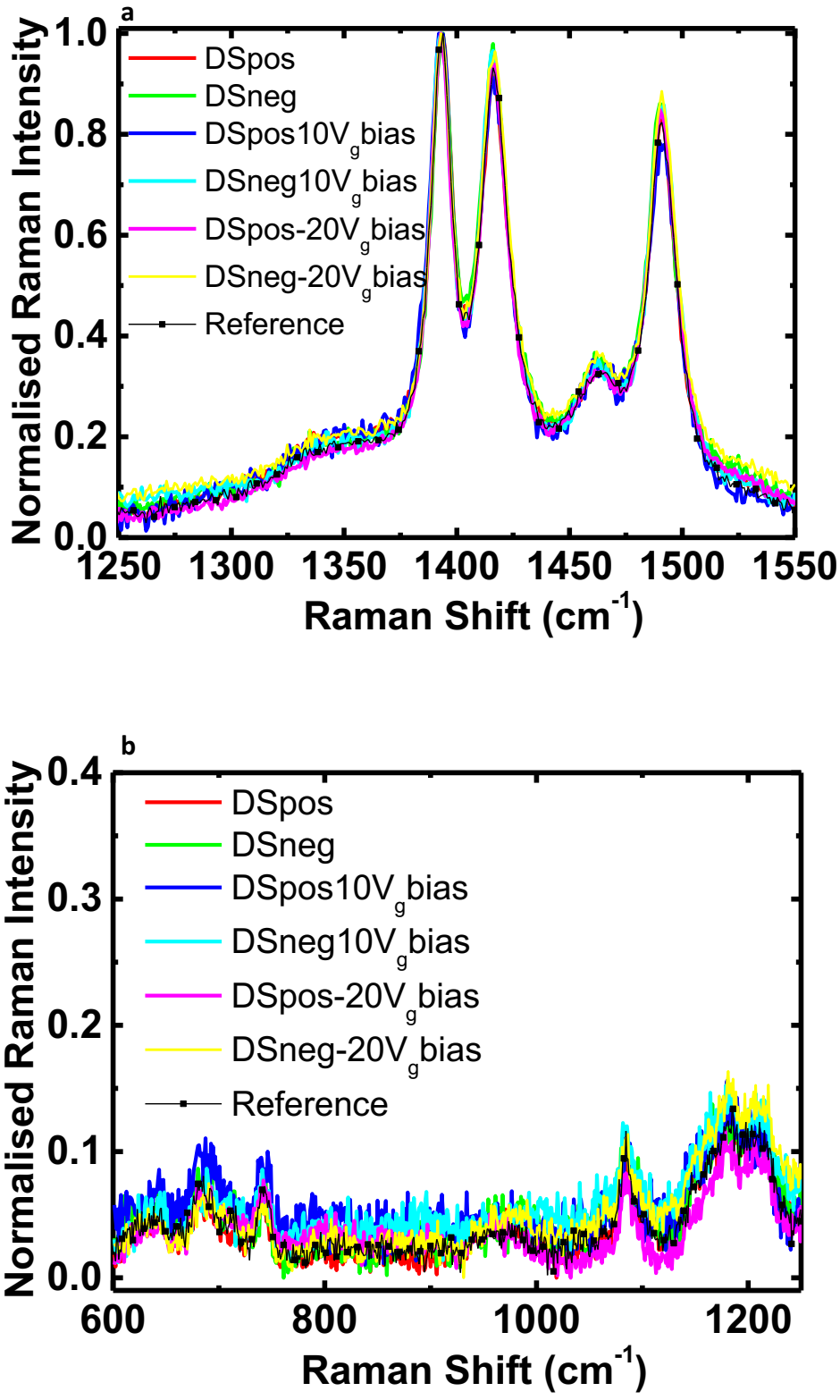


Figure 3-74: The 1250-1550 cm^{-1} (a) and the 600-1250 cm^{-1} (b) portions of the Raman spectra of the TLP tested PBTTT OFETs.

The portion 1250-1550 cm^{-1} of the PBTTT spectrum is characterised by the thiophene C-C stretch mode (C_β-C_β intra-ring stretching) at 1393 cm^{-1}, the thienothiophene C=C stretch mode (C_γ=C_γ intra-ring stretching) at 1418 cm^{-1}, the inter-ring C-C stretch mode (C_α-C_α inter-ring stretching) at 1463 cm^{-1} and the thiophene C=C stretch mode (C_α=C_β intra-ring stretching) at 1493 cm^{-1}[10],[169], [170]. The region of this portion within 1350 cm^{-1} and 1550 cm^{-1} is also referred as the C=C-C ring stretch region[10]. Such peaks are visible in Figure 3-74 (above).

The analysis of the portion 600-1250 cm^{-1} is characterised by the C-C inter-ring stretch mode (C_α-C_α stretching) at 1208 cm^{-1}, the C-H bending plus a C-C inter-ring stretch mode at 1180 cm^{-1}, the C-H bending mode at 1084 cm^{-1} and by the C-S-C ring deformation generating the peaks at 745 cm^{-1}, 689 cm^{-1} and 644 cm^{-1}[65], [170].

The analysis of the 1300-1550 cm^{-1} spectra show only negligible variations of the peaks within such range after the TLP and the same can be observed for the region 600-1250 cm^{-1}. Therefore, the overall molecular organisation is maintained regardless of the applied stress. This result shows a higher resiliency of PBTTT if compared with P3HT with regard to ESD phenomena.

3.2.3.4 *Discussion over Drain Source TLP tests*

The DSpos and the DSpos10$V_g$bias resulted the most damaging tests to PBTTT OFETs whereas the DSpos-20$V_g$bias tested devices maintained their functionality. Interestingly, the DSneg, the DSneg10$V_g$bias and the DSneg-20$V_g$bias did not cause a complete failure of the devices but significantly altered their functionality and lowered their electrical parameters. In fact, the OFETs tested according this latter suffered a reduction of the mobility of almost the 30 %, a reduction in module of the threshold voltage by 70 % and a tenfold reduction of the on/off ratio (Table 15).

In the DSpos and in the DSpos10$V_g$bias the I_{LEAK} follows linearly the I_{TLP} up to the trigger point and it start decreasing afterwards. This behaviour points out a progressive loss of electric transport over the device due to the destruction of the drain pad-interdigitated pattern metal connection. In the DSpos-20$V_g$bias, instead, the I_{LEAK} value instantaneously is reduced after the trigger point as a result of localised damages over the interdigitated pattern. In these three cases, the E_{TR} ranges between 3.5 µJ and 7.8 µJ pointing out that any positive pulse equal or higher in energy than 3.5 µJ permanently damages but not necessarily causes a complete failure of PBTTT OFETs.

The DSneg and DSneg-20$V_g$bias tests have similar outcomes in terms of measured E_{TR} and I_{LEAK} behaviour, with the first one found ranging between 0.65 µJ and 1.85 µJ and the second one following linearly the I_{TLP} up to the trigger point and keeping in increasing afterwards but no longer

linearly, as a result of the incipient loss of the electrical contact between the TLP-probe and the drain pad. These tests did not fatally damage the devices but caused an important grating of their electrical features. The mobility resulted more than halved and the on/off ratio suffered a tenfold reduction. Interestingly, the V_{TH} increased to almost 20 V in the DSneg test (Table 15). Although the devices keep their functionality their usability is compromised and therefore I can assume that a pulsed energy higher than 0.65 μJ is not tolerable for such devices.

The DSneg10$V_g$bias is instead fatal to PBTTT OFETs. The E_{TR} values registered in this test resulted the highest observed for the PBTTT OFETs, reaching values of almost 15 μJ. The I_{LEAK} linearly follows the I_{TLP} up to the trigger point to start decreasing afterwards due to the failure of the drain pad-interdigitated pattern metal contact.

The alteration of the electrical features of TLP tested devices, as already observed in P3HT OFETs and discussed in section 3.2.2.5, are consequences of an enhancement of *interface-trapped charges*, *fixed charges in oxide* and of *trapped charges in oxide*. PBTTT itself resulted poorly altered by the TLP tests, as observed in the Raman spectra, and therefore a dication formation and subsequent stabilisation as cause of trapped charges in the oxide is not supported by experimental results.

To understand the different behaviours so far observed of PBTTT OFETs it is crucial to analyse the position of the charges within the polymer at the moment of the pulse striking and also whether the PBTTT is acting as p or n semiconductor. In the DSpos test the applied pulsed field induces a vertical and a horizontal field at each replica. The horizontal one needs to overcome the vertical field to start conducing the pulsed current throughout the device, similarly to what observed in the case of the P3HT. The trigger point position is therefore affected by the channel length, resulting higher for longer channel lengths. Furthermore, as observed in the P3HT, the trigger point reaches the highest values recorded for the TLP tests on PBTTT OFETs. The DSneg test is affected by the slower reactivity of the polymer to negative pulses, since the electron mobility is lower than the hole one, and the horizontal field does not manage to overcome the vertical one. Nevertheless, the applied field causes a notable enhancement of the traps within the device moving the V_{TH} forward of 20 V roughly.

For an applied bias of -20 V on the gate the holes are attracted to the gate whilst electrons are concentrated towards the drain and the source contacts. In such conditions, the channel of the device is open. Positive applied pulses are therefore free to move through the channel and interestingly the devices are only partially damaged maintaining a good functionality afterwards.

The polymer is hence dissipating the incoming energy mostly letting the pulsed charges to flow away and only partially by heating the metal lines and itself. Upon applied negative pulses, instead, the pulsed charges are forced to move into a negative-charge-carriers depleted channel, and thus blocked by a barrier. The pulsed energy is hence mostly dissipated via heat over the drain pad and the polymer itself. As shown by the Raman spectra, PBTTT is not significantly affected by this test and reasonably the weakening suffered by the devices and observed into the post-TLP IV curves (Figure 3-70) is mostly due to a worsening of the metal lines conductivity.

For an applied bias of 10 V to the gate, the electrons are attracted to the latter whilst the holes are moved towards the drain and the gate contacts. Upon applied positive charges a barrier impedes the charges to flow through up to the point the applied field is such to cause a breakdown of the junction and an impulsive flow of current that causes the destruction of the metal lines. Such breakdown is caused by the pulsed field when overcomes the fixed field due to the gate bias. The I_{LEAK} corroborates such thesis because of its sudden change straight after the trigger point, similarly to what observed in the analogous case involving the P3HT. Upon applied negative pulses instead, the OFETs are forced to work as n-type FETs in forward configuration with the channel opened. This explains the high values of E_{TR} found in correspondence of this case due to the pulsed charges flowing through the device. However, the PBTTT as n-type transistor is not as efficient as p-type and therefore the pulsed charges are partially dissipated via heating so resulting fatal to the metal lines. Importantly, the mobility and consequently the polymer ability to readily react to pulsed charges, is important to insure a proper dissipation of the pulsed energy by letting this to be flown away rather be dissipated by heating the metal lines, whenever the channel is opened. For such reasons, PBTTT in the DSpos-20$V_g$bias conditions is more efficient of the P3HT in the same conditions since the latter slower reactivity causes the pulsed energy to be mostly dissipated via heat. This finding, together with the Raman spectra showing no significant changes into the PBTTT polymer after the TLP tests, underline an excellent resiliency of the PBTTT to the TLP stress.

The R_{TLP} was found to be between 0.74 kΩ (DSpos10$V_g$bias) and 2.2 kΩ (DSpos) whenever the applied pulses were positive between the drain and the source, with the higher values found for the DSpos test, similarly to P3HT OFETs. Upon negative applied pulses, instead, the R_{TLP} was found ranging between 2.3 kΩ (DSpos10$V_g$bias) and 5.95 kΩ (DSneg). These values are too high to use PBTTT OFETs as ESD protections. For the design of ESD protections suitable for these devices, the allowed maximum value of pulse amplitude must not exceed the critical value of 0.65 μJ, whereas, the I_{TLP} and the V_{TLP} are required to be maintained lower than 0.04 A and 102 V respectively.

3.2.4 **Conclusions**

I characterised the response to TLP tests of P3HT and PBTTT OFETs according six different TLP conditions obtained by combining three different applied bias to the gate of such devices, namely 0 V, 10 V and -20 V, and by applying both positive and negative drain-source pulses per each of these gate biases. Furthermore, I characterised the response to TLP pulses of both polarities applied between the drain and the gate of the OFETs leaving the source unconnected. The electrostatic discharges are particularly destructive whenever these involve the silicon oxide of the devices. The positive pulses between drain and gate pointed out a clear failure of the devices, with a massive increase of the current between these terminals. Instead, the negative ones did not highlight a clear failure of the devices, although the measure of the IV curves confirmed permanent damages also in this case. These tests point out the necessity to adopt ESD protection limiting the permitted pulsed energy applied across the drain and the gate to values lower than 2.6 μJ, i.e. the lowest trigger energy found.

The P3HT OFETs are weak to the drain-source TLP stress. For positive applied pulses, the TLP stress between the drain and the source resulted particularly damaging for the interdigitated patterns and the metal contacts regardless of the applied gate bias. I observed a snapback region in the I_{TLP}-V_{TLP} curves of P3HT OFETs with the trigger point scaling according to the channel length of these devices. The negative applied pulses, regardless of the applied bias on the gate, do not fatally compromise the functionality of the devices. However, the mobility of these devices is reduced up to the 6%, the threshold voltage module is lowered between the 7% and the 14% remaining negative and the on/off ratio is reduced from the 33% to 37%. These alterations are due to both an increased level of charge traps, hence affecting the substrates, and to an induced reduction of the molecular order and stability of the P3HT as demonstrated by the Raman spectra collected from all the TLP tested P3HT OFETs. I also repeated the drain-source TLP test with the gate grounded by maintaining the pulsed energy lower than the minimum value observed in correspondence of the negative applied pulses (0.45 μJ). I hence characterised the devices stressed in such way, finding out a tenfold lowering in the charge mobility and in the on/off ratio values of these devices along with a displacement towards positive values of the V_{TH}. I also assessed the effect of an annealing (90° for 40 minutes) on the TLP-stressed transistors finding that this treatment is not particular beneficial to the devices. Eventually, I washed away the polymer layer from the stressed TLP substrates and prepared devices using fresh P3HT over the stressed substrates. These devices resulted less

performing of the pristine ones, regardless of the new P3HT used. This test confirms that substrates are damaged by the TLP also for low levels of pulsed energy.

PBTTT OFETs resulted more resilient to the TLP stress and more efficiently dissipating the pulsed energy. The tests exploiting positive applied pulses resulted fatally damaging if combined with the gate grounded or the gate biased with a positive voltage. Interestingly, only minor damages were observed for positive applied pulses over devices with a negative bias applied to the gate. In fact, according to the latter case, the device channel is opened and the PBTTT dissipates the pulsed energy mostly by letting this flowing through the device and only partially by heating the substrate metal lines. In correspondence of the negative applied pulses and the gate kept grounded or biased with a positive voltage, the devices resulted heavy weakened and, despite maintaining their functionality, poorly performing afterwards. Instead, in the case of the gate biased with a positive voltage, the devices experienced a junction breakdown and a total failure. Interestingly, the Raman spectra did not show alterations to the TLP stressed PBTTT, confirming a superior resilience of such material respect to the P3HT.

The PBTTT superior tolerance to TLP stress stems from its significantly more crystalline structure. The linear conjugated co-monomer, thieno[3,2-b]thiophene, facilitates the adoption of the low-energy backbone conformation and hence provides more conformational back-bone stability. Furthermore, the low side-chain attachment density (half than in P3HT) permits interdigitation between the chains and the formation of stable and large three-dimensional crystalline domains[172]–[174].

Both P3HT and PBTTT OFETs feature R_{TLP} values close or higher than 1 kΩ, too high to suggest these devices as ESD protections. On the contrary, ESD protections need to be designed for these devices, following common criteria for protections between drain and source: maximum E_{TLP} of 0.65 μJ; maximum I_{TLP} of 0.037 A; maximum V_{TLP} of 102 V. Protections are also required between the gate and the drain/source, namely: maximum E_{TLP} of 3.4 μJ; maximum I_{TLP} of 0.2 A; maximum V_{TLP} of 168 V.

3.3 TLP test on F8BT OLEDs

I carried out TLP tests in three different bias conditions between the anode and the cathode of F8BT OLEDs: (i) positive and negative TLP with no bias between the anode and the cathode (ACpos and ACneg respectively), (ii) positive and negative TLP with a bias of 8 V between the anode and the cathode (ACpos8Vbias and ACneg8Vbias respectively), (iii) positive and negative TLP with a bias of 15 V between the anode and the cathode (ACpos15Vbias and ACneg15Vbias respectively). Each test was repeated on three different pixels, and thus the average values and the corresponding variance are calculated accordingly. Each graph here reported is representative for all the pixels treated in the same TLP-conditions. Devices are built and tested according procedure described in 2.4 and 2.5. In the following three sections the TLP parameters of the TLP-tested OLEDs, the OLED photo-electrical properties before and after the TLP test and a discussion over the results obtained are respectively reported.

3.3.1 OLED Parameters

In Table 21 are reported the V_{on}, the maximum emission wavelength (λ_{max}), the EQE and the maximum luminance (Max-L) of F8BT OLEDs before and after the ACpos TLP test. The values obtained from pristine F8BT OLEDs are comparable with reported works[175], [176]. An increase of approximately 0.5 V in the V_{on} of TLP-tested devices can be appreciated, as well as a slight red-shift of the λ_{max}. Importantly, a reduction of the EQE of approximately 85 % and of the Max-L of roughly 87 % are caused by the ACpos test, therefore permanent damages are induced by this test despite tested OLEDs maintained their functionality. The red-shift of the EL spectra with respect to the one collected from a pristine device is confirmed in Figure 3-75. Furthermore, broadening of spectra collected from TLP tested devices can be seen. The spectra of the pixel tested according the ACpos15Vbias test also present an alteration of the shape, probably due to contaminations of the active layer induced by diffusion of material from other layers of the devices due to the TLP creating cracks within the active layer. From graphs in Figure 3-76 we can see the JVL curves of ACpos tested devices. The LV graphs clearly show the shift causing the observed increase of the V_{on} of the devices, whereas the JV curve confirms that the current flowing within the device, for an applied voltage lower than the V_{on}, is much higher than the one that can be observed in the pristine curves. In Figure 3-77a, the EQE curves of ACpos tested devices can be seen. An important loss of such figure of merit is shown in this graph. Eventually, in Figure 3-77b, the JVL curves of the pixel that maintained its

Table 21: The photoelectrical parameters of F8BT TLP tested OLEDs.

	V_{on} (V)	λ_{max} (nm)	EQE (%)	Max-L (Cd/m^2)
Pristine	3.63±0.34	551±2	0.786±0.013	3492±507
After ACpos	4.01±0.17	554±5	0.113±0.028	439±98

functionality after the ACpos15Vbias test are shown. Although the device can be switched on, the V_{on} is shifted of almost 4 V ahead by comparison with the V_{on} of pristine devices and the shape of the LV curve is considerably altered. The JV curve also shows a higher current in comparison to the current measured in pristine devices. For instance, for an applied voltage of 2 V the current density of pristine devices is around 10^{-5} mA/cm^2 against a value of almost 100 mA/cm^2 in the ACpos15Vbias tested device.

Interestingly, during the ACpos tests, OLEDs were switched on by the applied pulses and their luminance increased with the pulse amplitude. The explanation lies in the pulsed charges recombination taking place within few nanoseconds, whilst the pulses elapse for ~100 ns, and in the generated pulsed field progressively involving a higher number of charges as its amplitude increases.

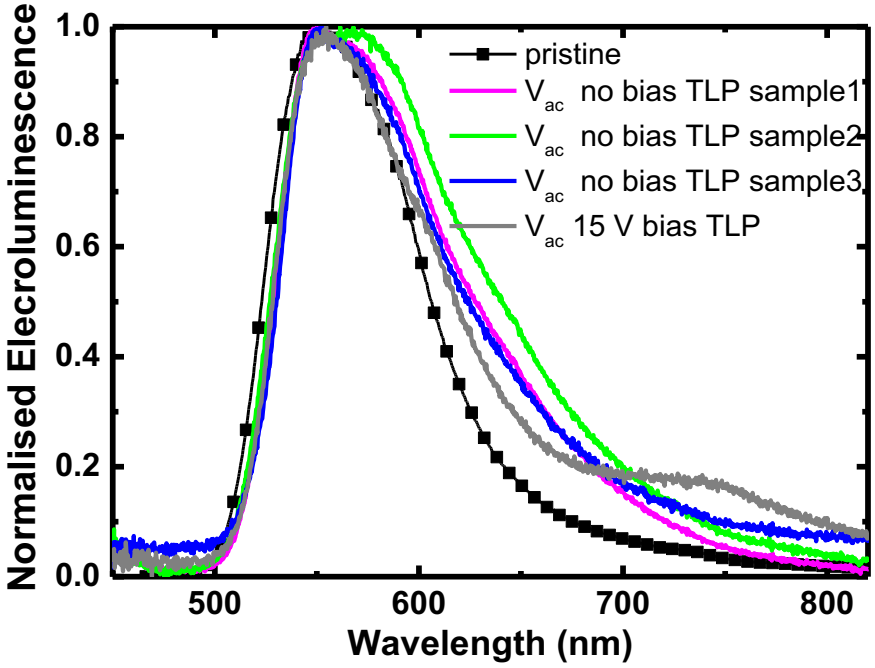


Figure 3-75: The EL spectra collected from the F8BT OLEDs tested according the ACpos and ACpos15Vbias TLP tests. Red-shift and broadening characterise spectra collected from TLP tested devices.

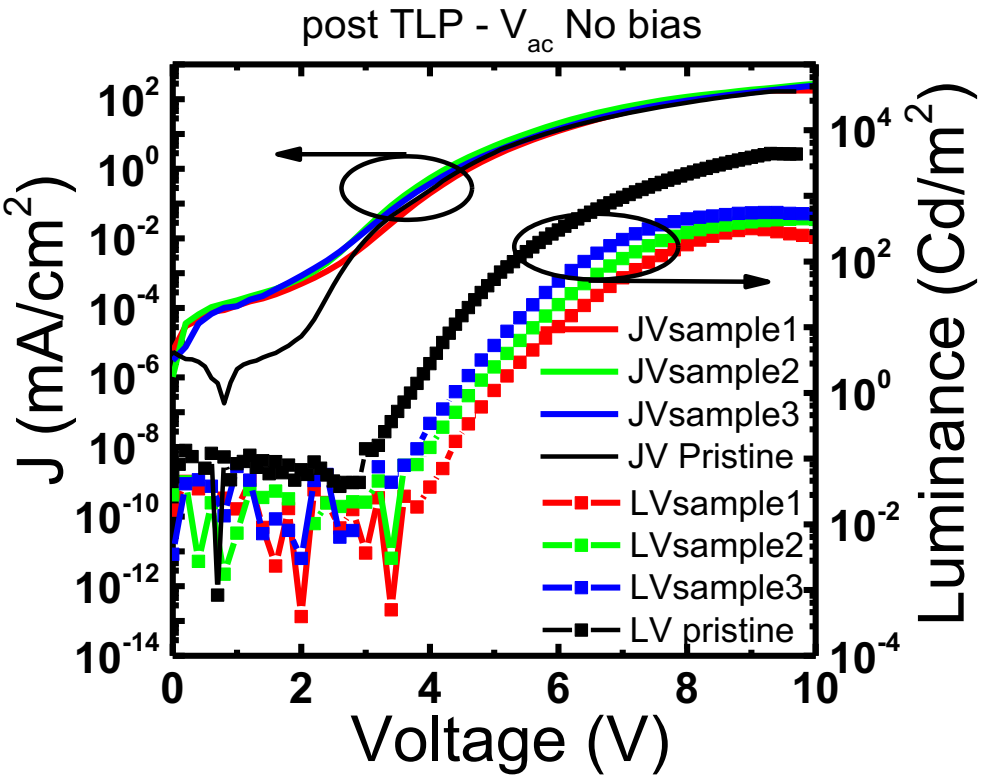


Figure 3-76: JVL graphs of ACpos tested devices.

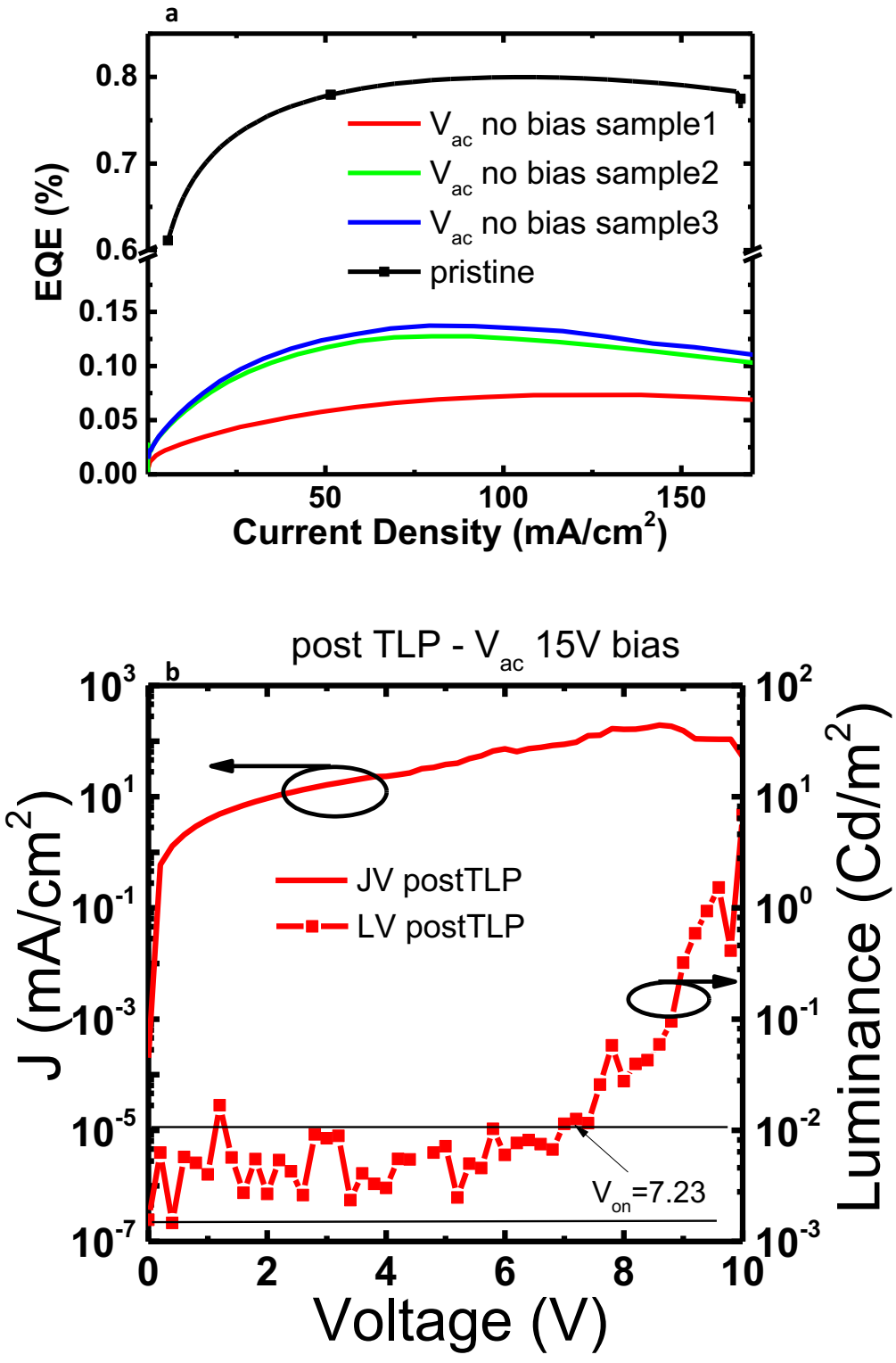


Figure 3-77: The EQE graphs of ACpos tested OLEDs (a) and the JVL graph of a pixel after the ACpos15V test (b).

3.3.2 **TLP test results**

The TLP failure criterion relies on the I_{LEAK} overcoming an I_{FAIL} of 10 mA (compliance current was set to 35 mA), measured for an applied V_{ac} of 4 V, in the case of the TLP test carried out with no V_{ac} bias applied, or 8 V in all other TLP tests. The DC test were obtained by applying a V_{ac} spanning between 0 V and 15 V (compliance current was set to 10 mA to avoid over heating of the device during the test). The ACpos TLP test did not cause the failure of the devices. All the other tests induce major damages of the OLEDs, which could not be switched on after the tests. An exception was observed in one of the device tested according the ACpos15Vbias test, which can be switched on after the TLP test, though major damages occurred as explained later. The TLP parameters obtained from all the TLP tests are reported in Table 22. The TLP graph of the ACpos and ACneg tests are depicted in Figure 3-78. In the ACpos TLP graph, the linearity of the I_{TLP} vs V_{TLP} curve is maintained throughout the test, which resulted limited by the TLP maximum pre-charge voltage (2000 V) allowed by the system. The I_{LEAK} decreases with the I_{TLP} increasing, up to a point in which it remains approximately the same. Such decrease can be ascribed to both an increase of the polymer conductivity, induced by heat, and to parasitic electric path arising during the test. Although the ACneg TLP curves show a certain degree of linear dependency between the I_{TLP} and the V_{TLP}, fluctuations due to punctual release of energy, similar to trigger points, can be observed. These cannot be classified as true trigger points since are not followed by snapback regions. Also in the ACneg test the system reached its maximum pre-charge voltage. However, in this case, the test causes permanent damages to the devices, therefore I chose the last measured value of the I_{TLP} and V_{TLP} as I_{TR} and V_{TR}, respectively.

Table 22: The TLP parameters obtained in correspondence of the three TLP tests carried out on F8BT OLEDs.

	V_{TR} (V)	I_{TR} (A)	E_{TR} (μJ)	R_{TLP} (Ω)
ACpos	x	x	x	98±3
ACneg	238±64	1.1±0.7	24.8±18	216±100
ACpos8Vbias	80±14	2.1±0.5	16.1±6	34.3±2
ACneg8Vbias	52±2	1.1±0.1	5.1±0.1	46.5±2
ACpos15Vbias	120±3	3.5±0.1	38.5±2.2	36.9±6
ACneg15Vbias	60±2	1.15±0.1	6.1±0.4	43.5±1

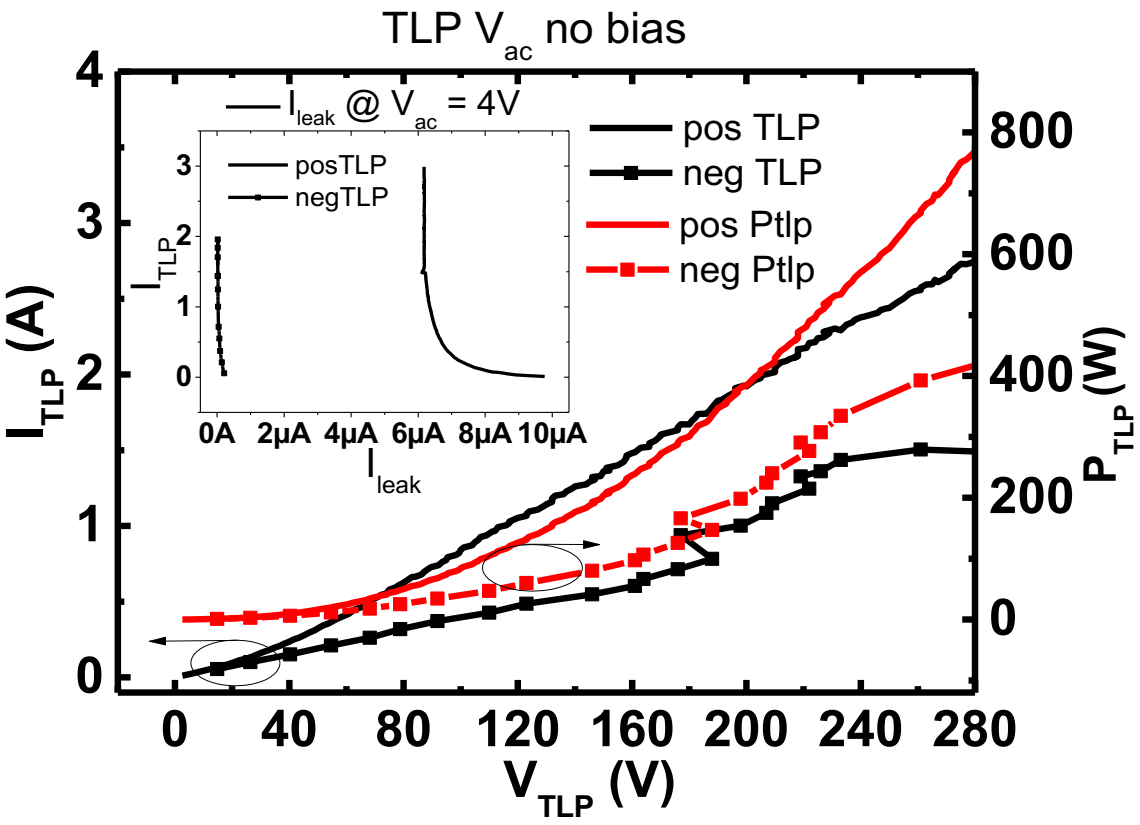


Figure 3-78: The TLP graphs of the ACpos and ACneg tests carried out on F8BT OLEDs.

In Figure 3-79 are reported the TLP graphs of the ACpos8Vbias and ACneg8Vbias tests. The I_{TLP} vs I_{LEAK} graphs reveal that in both cases the I_{LEAK} test was not passed, with the I_{LEAK} reaching values as great as 17 mA, by far higher than the set I_{FAIL}. The I_{LEAK} also suggests that the DUT conductivity is altered and increased because of the test, and thus new low-resistive paths arise into the device. Nevertheless, the failure does not trigger a short circuit into the devices. As seen in the ACneg tests, no proper trigger points can be observed in the I_{TLP} vs V_{TLP} graphs. Therefore, for both the ACpos8Vbias and ACneg8Vbias tests, I chose the last measured values from such graphs as the trigger values. In these two TLP modalities, the test was stopped within 5 steps from the sudden increase of the I_{LEAK}, taken as a sign of a permanent damage taking place in the devices. Therefore, the system did not reach the maximum pre-charge voltage value this time.

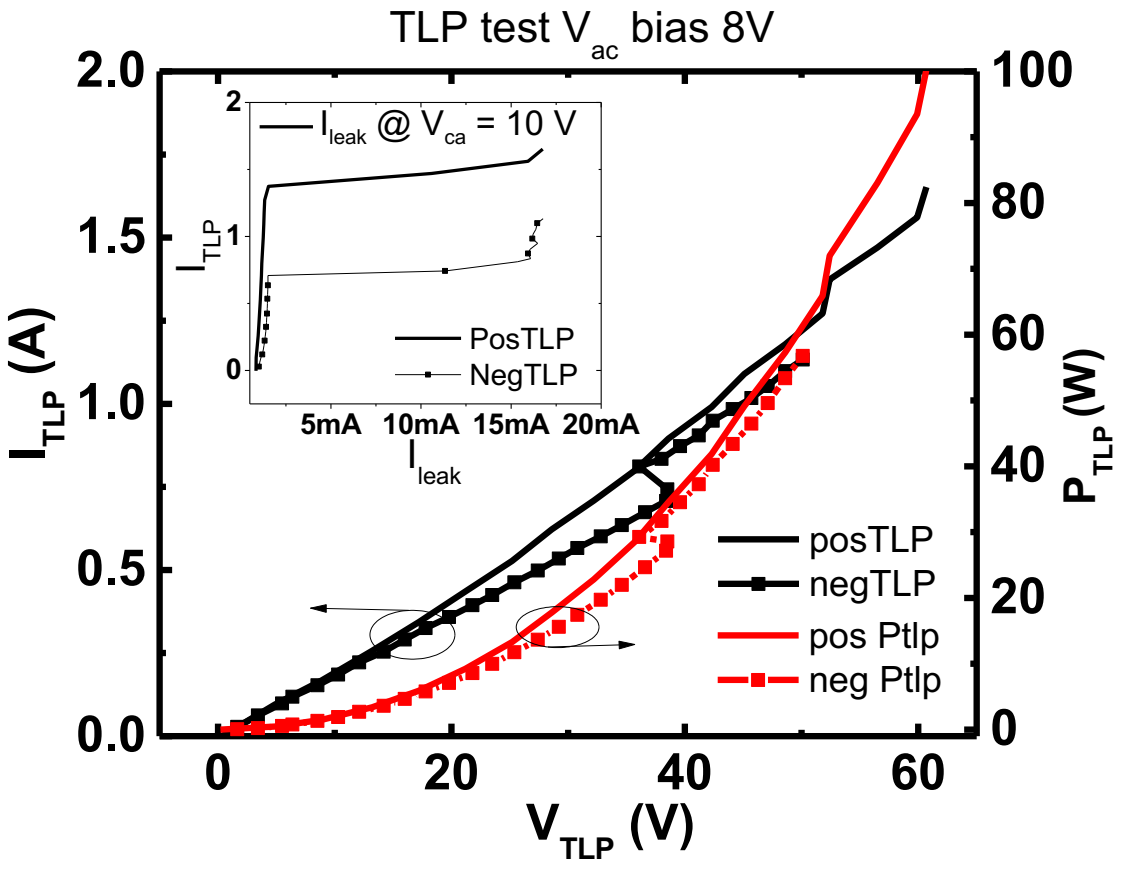


Figure 3-79: the TLP graphs of the ACpos8Vbias and ACneg8Vbias tests obtained from F8BT OLEDs.

In Figure 3-80 are reported the TLP graphs of the ACpos15Vbias and ACneg15Vbias tests. Interestingly, one of the pixel tested according the Acpos15Vbias test resulted still able to switch on and emit light, although its photoelectrical features are worsened. The other devices tested according this mode cannot be switched on anymore. The latter are characterised by an I_{LEAK} overcoming the I_{FAIL}, as a sign of permanent new low-resistive electric paths arisen within the device active layer, and taking place regardless of pulses polarity. However, in the ACpos15Vbias the failure occurs for a value of the pre-charge voltage very close to the maximum value allowed by the system, and in one case (the pixel switching on afterwards), no failure takes place. Instead, in the ACneg15Vbias the I_{LEAK} overcomes the I_{FAIL} for much lower values of pulsed energy. The ACpos15Vbias tests do not show proper trigger points, hence the last recorded values in the I_{TLP} vs V_{TLP} were taken as trigger values. On the contrary, the ACneg15Vbias curves show a trigger point followed by a short snapback region. No short circuits were observed because of the TLP tests.

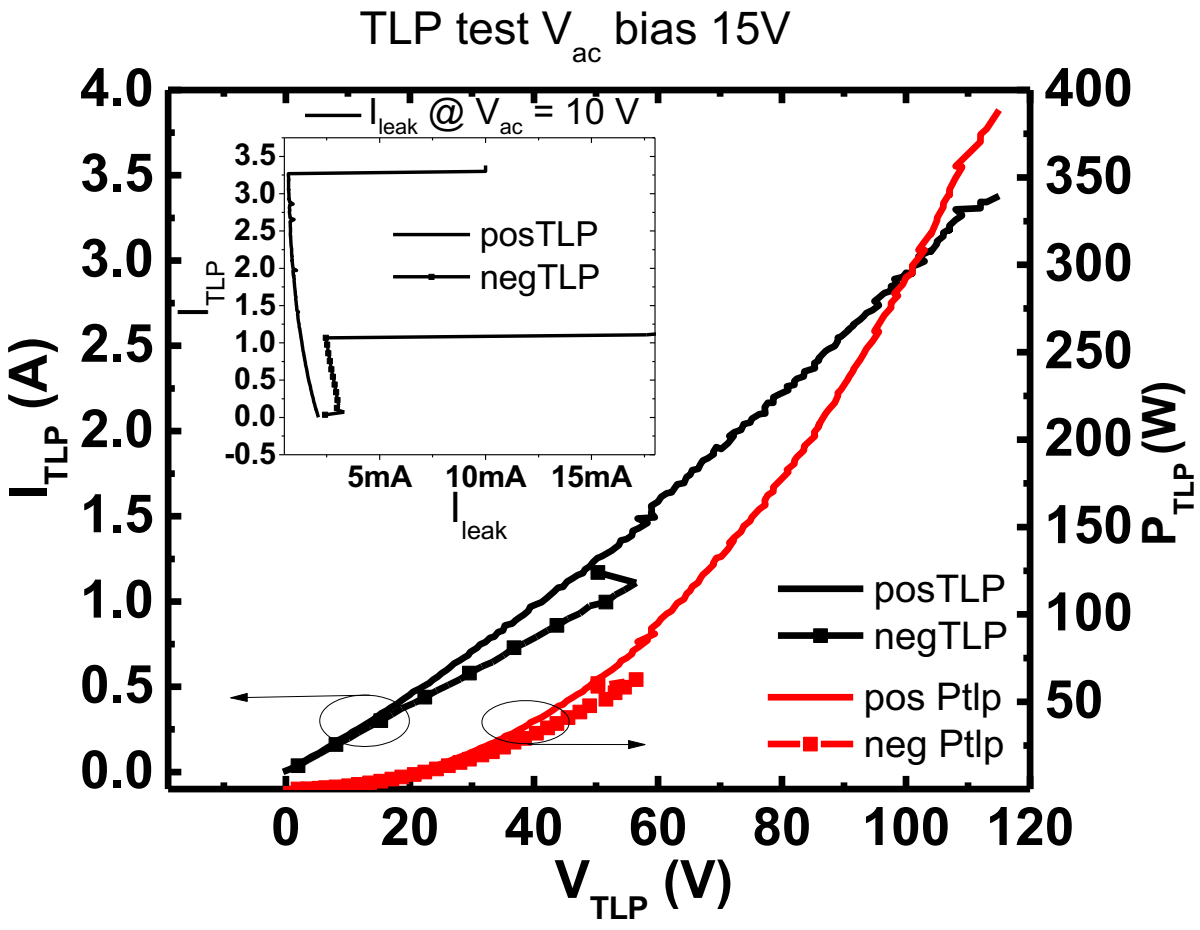


Figure 3-80: the TLP graphs of the ACpos15Vbias and ACneg15Vbias tests obtained from F8BT OLEDs.

The R_{TLP} is lower than 100 Ω in all the cases, except for the ACneg in which values as high as 316 Ω are reached. Reasonably, the tests in which positive pulses are deployed the resistance appears slightly lower than the respective negative counterpart. However, such differences result subtle in comparison to other polymer so far discussed (P3HT, PBTTT) due to F8BT having comparable value of charge mobility for both holes and electrons.

DC tests were carried out after each TLP test having the V_{ac} spanning from 0 to 15 V (Figure 3-81). The outcomes of these tests are similar regardless of the V_{ac} or polarity used, i.e. the current the device allows to pass is much higher than the one allowed to flow before the TLP test, underlining that the TLP tests favour the formation of low-resistance paths that discourage the formation of excitons within the device. In fact, the stress the devices undergo during the TLP stress creates path of low impedance between the electrodes due to migration of Ca particles from the cathode and/or PEDOT:PSS from the anode into the active layer, favoured by both the high temperature and the pulsed electric field. In the ACpos and the ACneg tests, the increase of the DC current is less marked, and devices maintain a semiconductor-like behaviour, instead in the other cases the behaviour is more metallic-like, meaning the applied bias further stimulates the arise of low-resistive paths so reducing the likelihood for injected charges to successfully recombine, and therefore making the active layer more and more metallic by lowering both γ and η_{PL} (Equation 1.8).

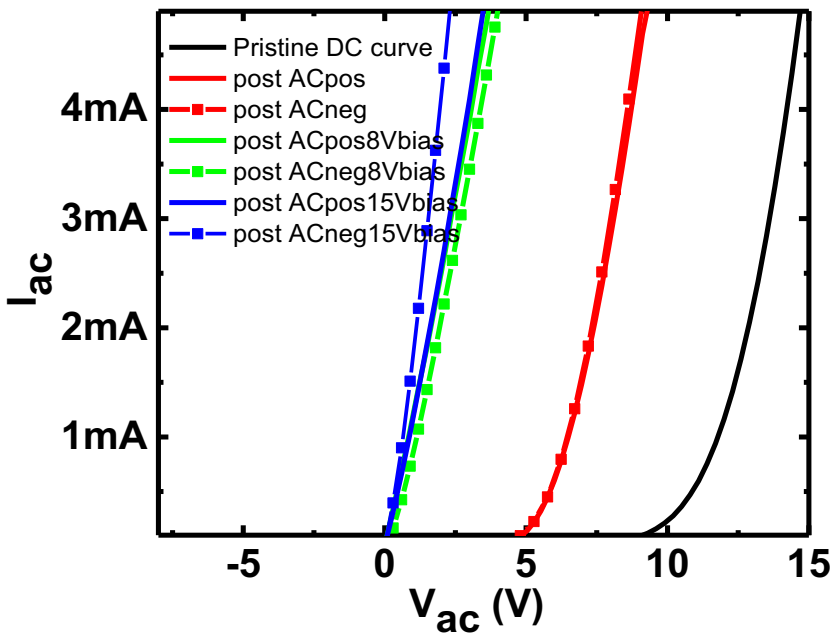


Figure 3-81: The DC curves measured after every TLP tests carried out on F8BT OLEDs.

3.3.3 **Discussion of the results of F8BT after TLP tests**

The ACpos test is the least damaging for F8BT OLEDs, which kept acceptable features afterwards. The reason lies in the efficiency of F8BT to discharge the pulsed current limiting the overheating of the device, and thus avoiding a molecular order alteration of the active layer. However, the TLP tests cause an increase of localised states within the polymer, because of charges remaining trapped within the polymer, which are responsible for the red-shift observed in the EL spectra (Figure 3-75) and for the increase of the current density[177], [178]. The HOMO-LUMO gap results lowered upon an induced increasing of localised states, therefore TLP tests act as electric doping to F8BT[179]. Looking at equation 1.8, I expect the reduction of the EQE (Table 21) mostly due to γ and η_{PL} factors, since F8BT molecular alterations also change the PL efficiency, and thus, the number of excitons forming within the device. In fact, low-resistive localised domains arise within the polymer, reasonably due to the increase of trapped charges because of the diffusion within the polymer of Ca and PEDOT:PSS molecules from electrodes, favoured upon formation of small cracks into the active layer heated up by the pulsed energy. Such low-resistive paths reduce the likelihood for injected charges to successfully recombine, and therefore make the active layer more and more metallic by lowering both γ and η_{PL}. This interpretation and the presence of such phenomena are corroborated by Figure 3-81 that shows how devices are changing their behaviour from semiconducting to metallic after the TLP tests, especially in tests involving a V_{ac} bias. However, further tests such as PL efficiency, time-correlated single-photon counting (TCSPC), and x-ray photoelectron spectroscopy (XPS), not carried out within the activities reported in this thesis, are required to shed light on this aspect.

With no applied bias between the anode and the cathode, as in ACpos and ACneg tests, charges are evenly spread throughout the polymer along the direction between the two electrodes. Upon an applied pulse, the pulsed electric field moves the charge carriers according the pulse polarity. F8BT, featuring both a good electron and hole mobility, causes the I_{TLP} vs V_{TLP} graphs to appear reasonably linear regardless of the polarity used for the ACpos and ACneg TLP test. However, the lower electron mobility featured by this material causes the negative pulses to result more damaging, as corroborated by the lower values of trigger energy and by the higher values of R_{TLP} observed in correspondence of ACneg tests (Table 21), with respect to the positive counterpart, and thus, confirming that a higher degree of energy dissipation and heating unfolds in the ACneg tests.

When the devices are biased with a positive V_{ac} bias and interested by positive pulses, the pulsed charges are partially involved in the recombination process, therefore releasing their energy and

contributing in the total emission of light from the OLEDs. Thence, pulsed charges only partially are dissipated via heat, so triggering polymer chains reconfiguration and small cracks formation. With the applied V_{ac} bias increasing, the number of pulsed charges involved into recombination and light emission increases, therefore the mean trigger energy results 58% higher in the ACpos15Vbias in comparison with the one observed in ACpos8Vbias tests. Upon applied negative pulses over positively biased devices, the pulsed charges generate a field that is opposite to the one moving the charges within the polymer, hence the recombination process is perturbed. The pulsed charges are mostly remaining confined close to the electrodes of the devices, therefore cannot be efficiently dissipated and the polymer is heated up. The response to the negative pulses is similar for both V_{ac} bias values used.

Interestingly, F8BT OLEDs feature low values of R_{TLP} in all tests, remaining always lower than 316 Ω and lower than 50 Ω in 4 out of 6 carried out tests. Therefore, these devices could act as ESD protection as well. In case ESD protections need to be designed for these devices, E_{TR} must be maintained as low as 5.6 μJ, whereas the I_{TLP} and the V_{TLP} cannot overcome 1 A and 50 V, respectively. Nevertheless, these values are very high and point out an excellent robustness to ESD stress featured by F8BT OLEDs.

3.3.4 **Conclusions**

I tested F8BT OLEDs in three different operating conditions, i.e. when no bias is applied between the anode and the cathode and when the OLEDs are on according a bias of 8 V and of 15 V. Interestingly, no trigger points at all were observed in the case of positive pulses applied over no-biased devices, which could be switched on after the TLP tests. However, we found TLP tests increasing the V_{on} of almost 0.5 V and altering the JV curves of these OLEDs, i.e. increasing the overall current flowing through the devices, reasonably due to the formation of low-resistive path induced by diffusion of Ca and PEDOT:PSS molecules within the active layer, upon formation of small cracks within the bulk of the latter. So diffused molecules generate trapped charges that lower the HOMO-LUMO gap of devices causing the red-shift of the EL curves as well. One of the pixel biased with 15 V between anode and cathode and tested with positive pulses could also be switched on after the test. However, its photoelectric features resulted particularly worsened, as its V_{on} that from a pristine value of 3.6 V eventually resulted as high as 7.23 V. All the other tests caused the failure of the devices, which turned over a resistive behaviour afterwards. Therefore, TLP tests enhance the conductivity of the active layer of devices forcing them to lose a junction-behaviour and such

procedure is more remarkable in devices biased and tested with negative pulses. Nonetheless, the TLP parameters found for F8BT OLEDs reveal an excellent robustness to ESD events featured by these devices These, due to low value of R_{TLP}, can also be used as ESD protections.

3.4 Chapter Conclusions

In this chapter, I characterised the response to TLP stress of three different organic devices, namely OPVs, OLEDs and OFETs.

I tested P3HT:PCBM OPVs according positive and negative pulses. OPVs tested by means of positive pulses withstand currents higher than 3 A, dissipating an incoming power higher than 800 W without incurring into permanent damages. Furthermore, the photovoltaic parameters of such devices result improved with a final η increased of roughly 14% respect to the pristine ones. On the other hand, the same devices resulted much weaker in the case of negative applied pulses. Interestingly, OPVs can act as ESD protections, seen the values of R_{TLP} spanning between 10 Ω and 214 Ω. Otherwise, OPVs protections must avoid incoming ESD to overcome a pulsed energy of 0.32 μJ, an I_{TLP} of 0.13 A and a V_{TLP} of 29 V.

I characterised the response to TLP tests of P3HT and PBTTT OFETs according six different TLP conditions obtained by combining three different applied bias to the gate of such devices, namely 0 V, 10 V and -20 V, and by applying both positive and negative drain-source pulses per each of these gate biases. Furthermore, I characterised the response to TLP pulses of both polarities applied between the drain and the gate of the OFETs leaving the source unconnected. The electrostatic discharges are particularly destructive whenever these involve the silicon oxide of the devices, pointing out the necessity to adopt ESD protections. Tests involving the drain and the source resulted particularly damaging for the interdigitated patterns and the metal contacts, regardless of the applied gate bias. A snapback region in the I_{TLP}-V_{TLP} curves of both P3HT and PBTTT OFETs were observed. The negative applied pulses, regardless of the applied bias on the gate, do not fatally compromise the functionality of the devices. However, the mobility, the threshold and the on/off ratio of these devices result particularly affected and worsened. These alterations are due to the synergistic effect of an increased level of charge traps, hence affecting the substrates, and of an induced reduction of the molecular order and stability of the semiconducting polymer. However, Raman spectra collected from all the TLP tested OFETs show a higher resiliency of PBTTT OFETs with respect to the TLP stress thanks to its significantly more crystalline structure. Both P3HT and PBTTT OFETs feature R_{TLP} values close or higher than 1 kΩ, too high to suggest these devices as ESD

protections. On the contrary, ESD protections need to be designed for these devices, following these criteria for the drain and source: maximum E_{TLP} of 0.65 μJ; maximum I_{TLP} of 0.037 A; maximum V_{TLP} of 102 V. Protections are also required between the gate and the drain/source, namely: maximum E_{TLP} of 3.4 μJ; maximum I_{TLP} of 0.2 A; maximum V_{TLP} of 168 V.

I tested F8BT OLEDs in three different operating conditions, i.e. when no bias is applied between the anode and the cathode and when the OLEDs are switched on according a V_{ac} bias of 8 V and of 15 V. F8BT OLEDs tested with positive pulses and with no applied bias maintained their functionality. However, I found TLP tests increasing the V_{on} of almost 0.5 V and altering the JV curves of these OLEDs. Furthermore, the red-shift of the EL curves takes place. One of the pixel biased with 15 V between anode and cathode, and tested with positive pulses, could be switched on after the test. However, its photoelectric features resulted particularly worsened. All the other tests caused the failure of the devices, which turned over a resistive behaviour afterwards. Therefore, TLP tests enhance the conductivity of the active layer of devices forcing them to lose a junction-behaviour. Such procedure is more evident in devices biased and tested with negative pulses. Nonetheless, the TLP parameters found for F8BT OLEDs reveal an excellent robustness to ESD events of these devices that, due to low value of R_{TLP}, can also be used as ESD protections.

4. Neutron Aging of OPVs and OFETs

The mechanical (strength-to-weight ratio, lightweight, flexibility) and electrical properties organic semiconductors are known for[5], [180], combined with cheap and large-area manufacturing possibilities, have turned such materials compelling for spacecraft and aircraft applications. Polymers have been extensively employed in avionics as passive structural components[181], [182]. For instance, the necessity to exploit flexible materials for satellites was firstly explored in 1967 by Crabb et al. by using thinned Si wafers[183]. However, in such scenarios, the robustness against exposure to neutrons irradiation is one of the determining criteria for the choice of the materials eventually used to build spaceships, aeroplanes or even mini-satellites or weather-balloons[184], [185]. it is estimated that equipment on the International Space Station (ISS) receive an annual dose of ~$2.8x10^{11}$ neutrons/cm^2 (secondary neutrons generated by the interaction of cosmic rays with the Station vs. $3.85x10^5$ neutrons/cm^2 at ground level), with energies from 10^{-1} to 10^{11} eV[43], [139]. In such context, also ESD phenomena can take place affecting the equipment used in spaceships and aeroplanes[186]. In fact, ESD charging and discharging phenomena may lead to interferences with communication and navigation systems. Furthermore, ESD also generates electric field and voltages transients that could result fatal to electronic components and systems. ESD protections are normally used to prevent such occurrences. However, neutrons irradiation affects equally all circuits and components on board, including ESD protections. Therefore, the characterisation of the response to both ESD and neutrons irradiation of electronic circuits and materials used in such environments becomes very important. Interestingly, few studied so far have been published regarding conjugated polymer-based devices exposed to neutrons irradiation and all of them were obtained within the joint research carried out by Dr. Paternò, Dr. Garcia-Sakai and Prof. Cacialli[10], [22], [43], [119]. In fact, Paternò et al. reported for the first time about the effects of neutrons irradiation on P3HT and PBTTT OFETs[10]. In such work, the degradation of electrical parameters of these devices were investigated and reported, along with X-rays and Raman analysis. No studies at all, at the best of my knowledge, were reported about the combination of both ESD and neutrons irradiation on semiconducting polymer-based devices.

In the first section of this chapter, I report on the results I obtained by carrying out DSpos TLP tests (see 3.2.2.3.1) over P3HT OFETs that were previously exposed to three different neutron doses, or neutron hardening periods, namely 4 hrs, 12 hrs and 24 hrs. TLP parameters are reported along with

Raman Spectra collected from samples exposed to neutrons irradiation and the samples exposed to neutrons irradiation and TLP stress. In the second section, I report about the results I obtained by monitoring the photovoltaic features degradation of P3HT:PCBM BHJ solar cells neutron irradiated in operando conditions. The devices discussed in these two chapter-portions were fabricated and characterised according the procedure described in sections 2.2 and 2.3, whereas the TLP tests were performed as described in section 2.5. Raman spectra of P3HT OFETs were obtained by following the methodology described in section 2.6.2. The neutrons irradiation exposure of both P3HT OFETs and P3HT:PCBM OPVs were obtained in the VESUVIO beamline within the RAL laboratories. The neutrons energy spectrum featured by this beamline is described in section 2.7.

At the best of my knowledge, the work regarding the combined effects of TLP stress and neutrons irradiation on P3HT OFETs is the first one reported. Analogously, the in-operando neutrons hardening tests of OPVs here described are the first one of this kind reported.

4.1 ESD effects over P3HT neutron aged OFETs

I carried out DSpos TLP tests over P3HT OFETs that were previously neutrons hardened according three different aging periods, namely 4 hrs (T1), 12 hrs (T2), and 24 hrs (T3). In the first part of this section I report on the IV curves of P3HT OFETs prior the TLP treatment, whereas in the second part I report on the TLP parameters I obtained from these devices. In the third portion, I report on Raman analysis I carried out on neutrons aged P3HT OFETs before and after the TLP treatment. The results reported for each of the three cases treated (DSpos on P3HT OFETs neutrons aged according T1, T2, T3) were obtained out of three devices tested under the same conditions.

According the energy spectrum of neutrons generated within the VESUVIO beamline (2.7), the quantity of neutrons characterised by an energy of 10 MeV irradiating a sample in 6 minutes is equivalent to the same number of neutrons with same energy irradiating on equipment on ISS in 1 year. Therefore, a T1 dose is equivalent to an exposure of 40 years over ISS, whereas T2 and T3 are equivalent to 120 years and 240 years, respectively.

4.1.1 OFET parameters

I characterised neutrons hardened P3HT OFETs and obtained the IV curves and the electrical parameters of these before carrying on the DSpos test thereof. The neutrons aging process greatly reduces the performances of these devices, especially in those aged according T2 and T3 doses. The IV curves of the devices after each of the dose they were exposed, measured in correspondence of

V_{GS}=-80 V and V_{DS} spanning from 0 V to -80 V as regards the output characteristics, and for V_{DS}=-80 V and V_{GS} spanning between 10 V and -80 V as regards the transfer characteristics, are reported in Figure 4-1. The charge mobility, the threshold voltage and the on/off ratio of these devices are reported in Table 23. From both the curves and the parameters reported, we can understand that pristine devices undergone T1 are interested by a great loss of their figures, in particular the on/off is reduced of more than times, the mobility suffers of a tenfold reduction, whereas the V_{TH} mean value is moved towards the 0 of almost 6 V. Passing from T1 to T2, the figures are further reduced, in particular the mobility mean value is reduced of a another 80%, the curves shape are characterised by lower values of current, the V_{TH} mean value closes to the 0 of another 4 V and the on/off is reduced of a further 18 %. From T2 to T3 the figures suffer another remarkable values displacement, only the mobility is practically remaining the same. In fact, the V_{TH} was found moved ahead of another 5 V, reaching a value of -2.1 V, whereas the on/off is equal to 21.7 now, an order of magnitude lower than the one found for T2. Importantly, the values were measured out of only one of the three samples that were treated according T3, inasmuch the other two failed in showing any transistor behaviour. The curves in Figure 4-1 show a further reduction of currents.

Table 23: The electrical parameters obtained out of the P3HT OFETs neutrons hardened according three different aging periods, i.e. 4 hrs (T1), 12 hrs (T2) and 24 hrs (T3). OFETs aged according T3 resulted particularly damaged and parameters were inferred only from one sample.

DUT	Mobility ($x10^{-3}$ cm^2/Vs)	V_{TH} (V)	On/Off ($x10^4$)
Pristine	6.9±0.01	-17.4±5.2	0.9±0.16
T1	0.72±0.01	-11.8±2.3	0.022±0.003
T2	0.124±0.01	-7.2±1.3	0.018±0.002
T3	0.11	-2.1	0.0021

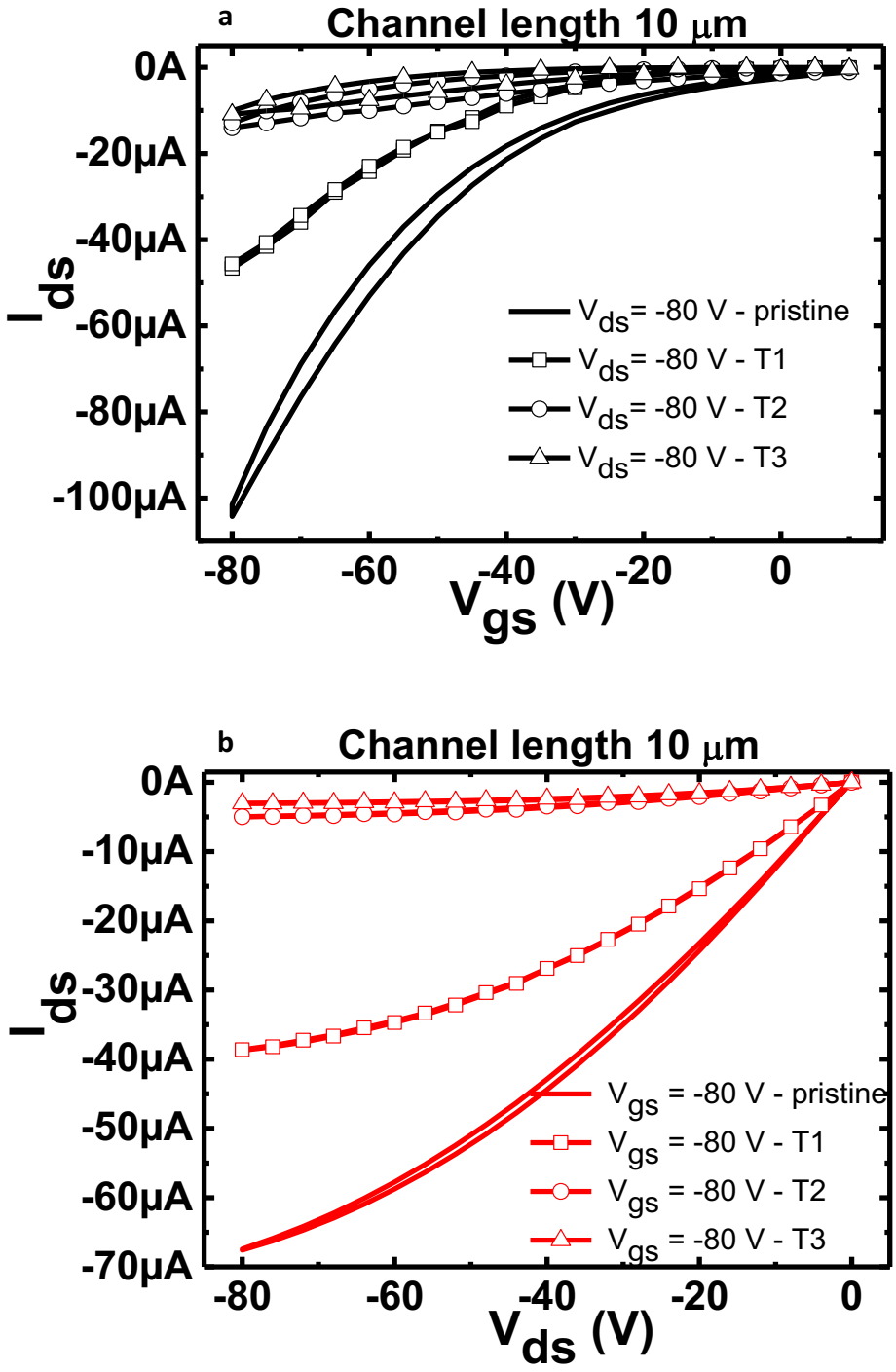


Figure 4-1: The transfer characteristics measured for an applied V_{DS} of –80V (a) and the output characteristics measured for an applied V_{GS} of -80V (b) of 10 μm channel-length neutron-hardened P3HT OFETs according three different aging periods, i.e. 4 hrs (T1), 12 hrs (T2) and 24 hrs (T3).

4.1.2 **TLP results**

The failure criterion chosen is the same used for the DSpos test carried out on P3HT OFETs analysed in section 3.2.2, namely I_{FAIL} = 0.5 mA. The I_{LEAK} was measured in correspondence of an applied V_{DS} of -20 V and an applied V_{GS} of -40 V. DSpos test exploits positive pulses between the drain and the source of the device, while the gate contact is grounded. Failure occurred in all devices tested according the DSpos test. In Table 24 are reported the TLP parameters obtained out of each DSpos-tested devices. T1 treated devices, as shown in Figure 4-2, are characterised by a snapback region and the TLP parameters obtained can be compared to those obtained out of P3HT OFETs that were not previously neutron aged, as described in 3.2.2.3.1. However, OFETs treated according T2 and T3 do not feature a snapback region (Figure 4-3), therefore I assumed as trigger point for these devices the first reduction in the I_{TLP} vs V_{TLP} curve equal or higher than -20%.

Table 24: The TLP parameters obtained out of P3HT OFETs tested according the DSpos mode that were previously neutrons hardened according three different aging periods, i.e. 4 hrs (T1), 12 hrs (T2) and 24 hrs (T3).

Dose	C. L. (µm)	I_{TR} (mA)	V_{TR} (V)	P_{TR} (W)	E_{TR} (µJ)	R_{TLP} (kΩ)
T1	20 µm	254.4±16	368±4	93.8±7.2	8.05±0.62	5±1.4
	10 µm	71.6±43	363±5	26±16.4	2.2±0.14	4.5±0.4
	5 µm	70.2±37	317±5	22.3±1.5	1.9±0.13	4.7±0.2
T2	20 µm	5.67±1	68.9±18	0.4±0.2	0.033±0.02	10.3±2
	10 µm	5.1±3	108.2±21	0.55±0.5	0.047±0.04	21.6±2.2
	5 µm	6.5±2	103.4±17	0.67±0.4	0.058±0.03	15.7±2.4
T3	20 µm	3.1±1	76.4±15	0.24±0.2	0.023±0.01	21±3.1
	10 µm	5.4±2	77.3±13	0.42±0.2	0.036±0.02	14.5±4.2
	5 µm	5.1±2	107.4±13	0.54±0.2	0.046±0.02	21.3±5

TLP parameters reveal how T2 and T3 dramatically reduce P3HT OFETs robustness to TLP stress. In fact, the minimum E_{TR} value found for T1 treated OFETs is 3.1 µJ, whereas in T2 and T3 treated devices such parameter plummets to 0.13 µJ and 0.11 µJ, respectively. Also, R_{TLP} is importantly different between T1 and T2-T3 treated P3HT OFETs, as in the first case its value ranges between 1.1 kΩ and 4.4 kΩ, whilst in the second and the third cases the range is between 8 kΩ and 26 kΩ. Such high values of resistance induce the pulses to discharge their energy almost entirely via heat.

The I_{LEAK} curves of T2 and T3 treated devices do not show any linear behaviour, this underlines that since the first applied pulse the devices start suffering permanent damages, despite the trigger point displaying usually around the 6^{th}-7^{th} applied pulse. Furthermore, I_{LEAK} remains very low in all cases analysed, i.e. under 10 µA, therefore P3HT is greatly altered by neutrons irradiation T2 and T3, resulting very restive to the I_{LEAK} stimulation.

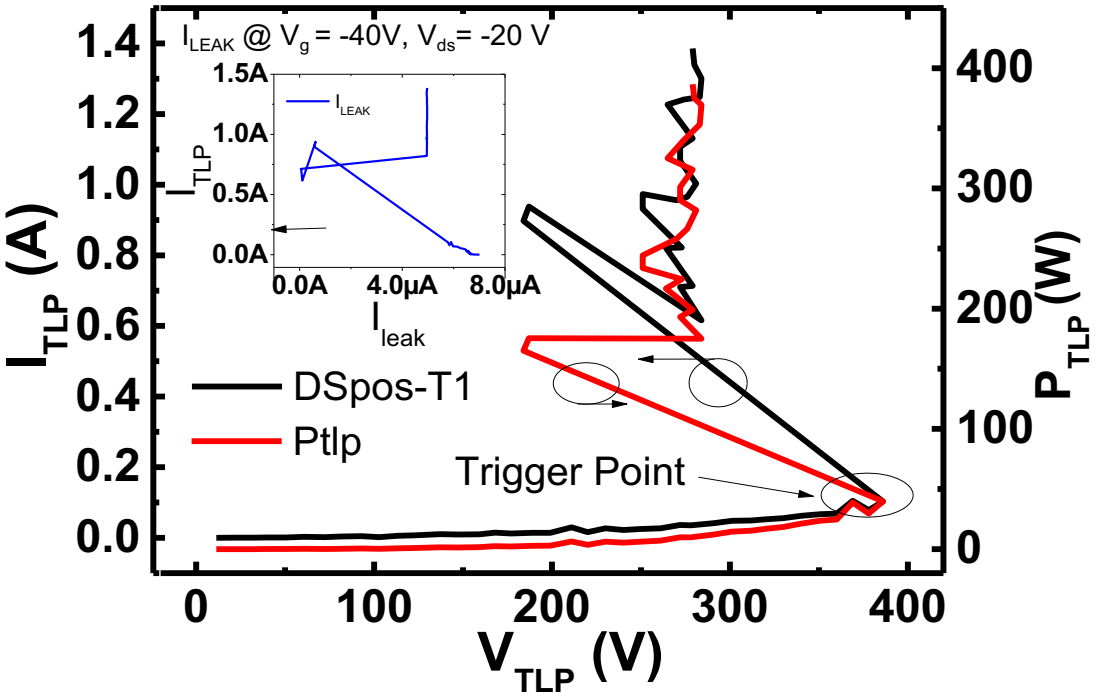


Figure 4-2: The TLP curves of a 10 µm channel length P3HT OFET neutron aged according a period of 4 hrs.

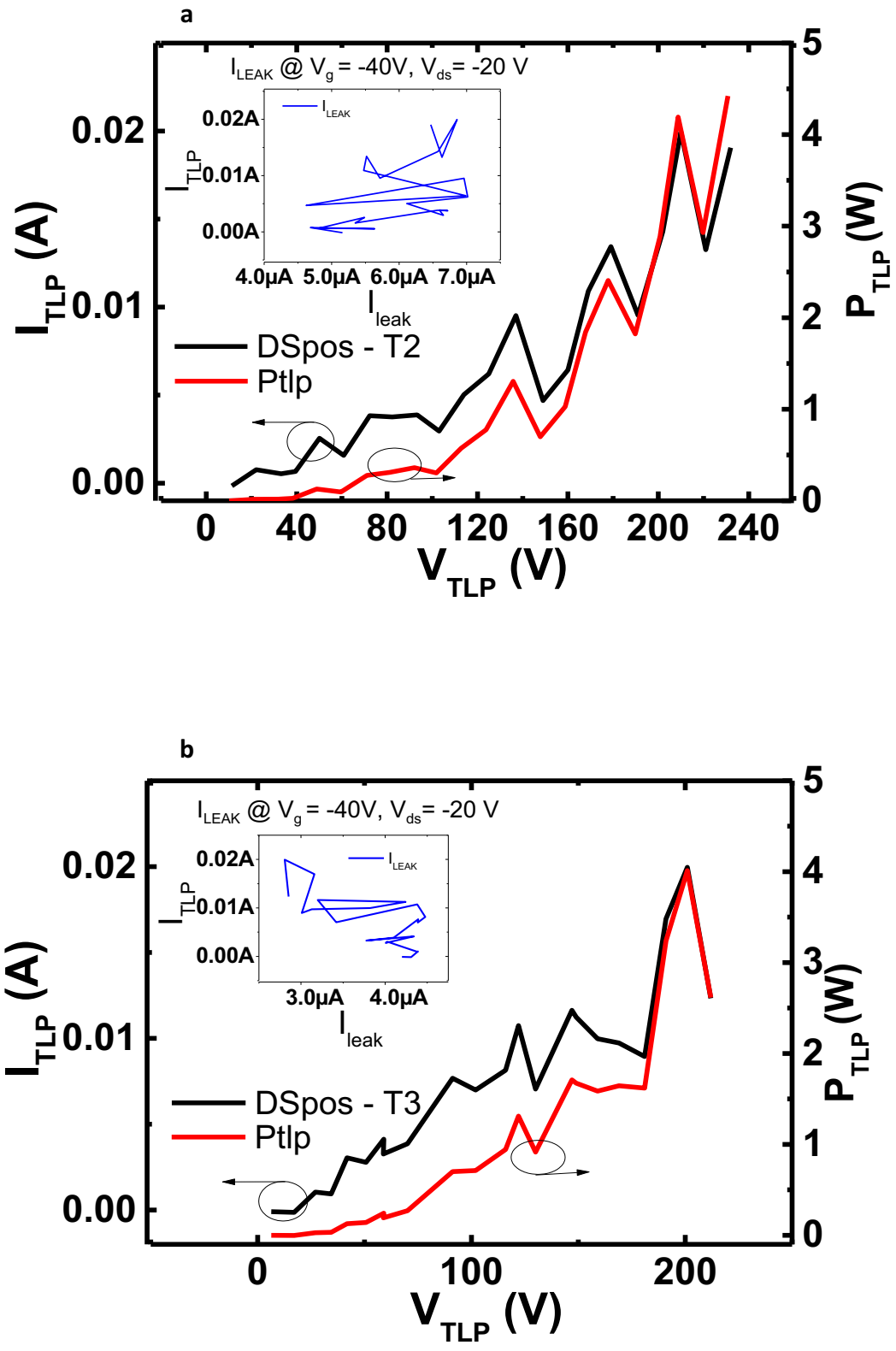


Figure 4-3: The TLP curves of 10 μm channel length P3HT OFETs neutron aged according a period of 12 hrs(a) and 24 hrs (b). No snapback region is present and the I_{LEAK} has a random behaviour.

4.1.3 **Raman Investigations**

The Raman spectra were collected from each of the tested devices and compared with reference spectra taken from a pristine device. Spectra are normalised respect to the peak at 1445 cm^{-1}, generated in P3HT spectra by the stretching of the in plane double bond C=C (C_α=C_β stretching). Representative spectra per each dose used, taken before and after the DSpos treatment, were chosen and reported in Figure 4-4. Such graph is then split in two other graphs, in the first one the portion 1250 to 1550 cm^{-1} of the original spectra is analysed (Figure 4-5a), whilst the portion 600 to 1300 cm^{-1} is analysed in the second one (Figure 4-5b). The mechanical vibrations of the molecular bonding are described referring to the α- and β- positions [166] of carbons within the thiopene rings composing the polymer, as done in section 3.2.2.4 (Figure 3-42).

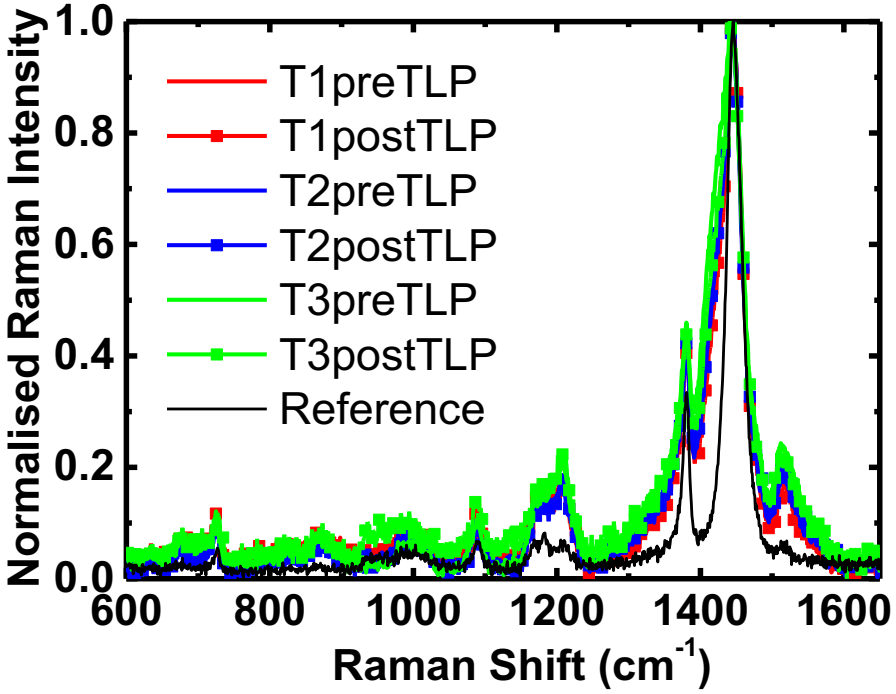


Figure 4-4: The normalised Raman spectra, within the range 600-1700 cm^{-1}, of P3HT OFETs that have undergone neutrons aging according three different doses (T1=4 hrs, T2=12 hrs, T3=24 hrs) and DSpos TLP stress test.

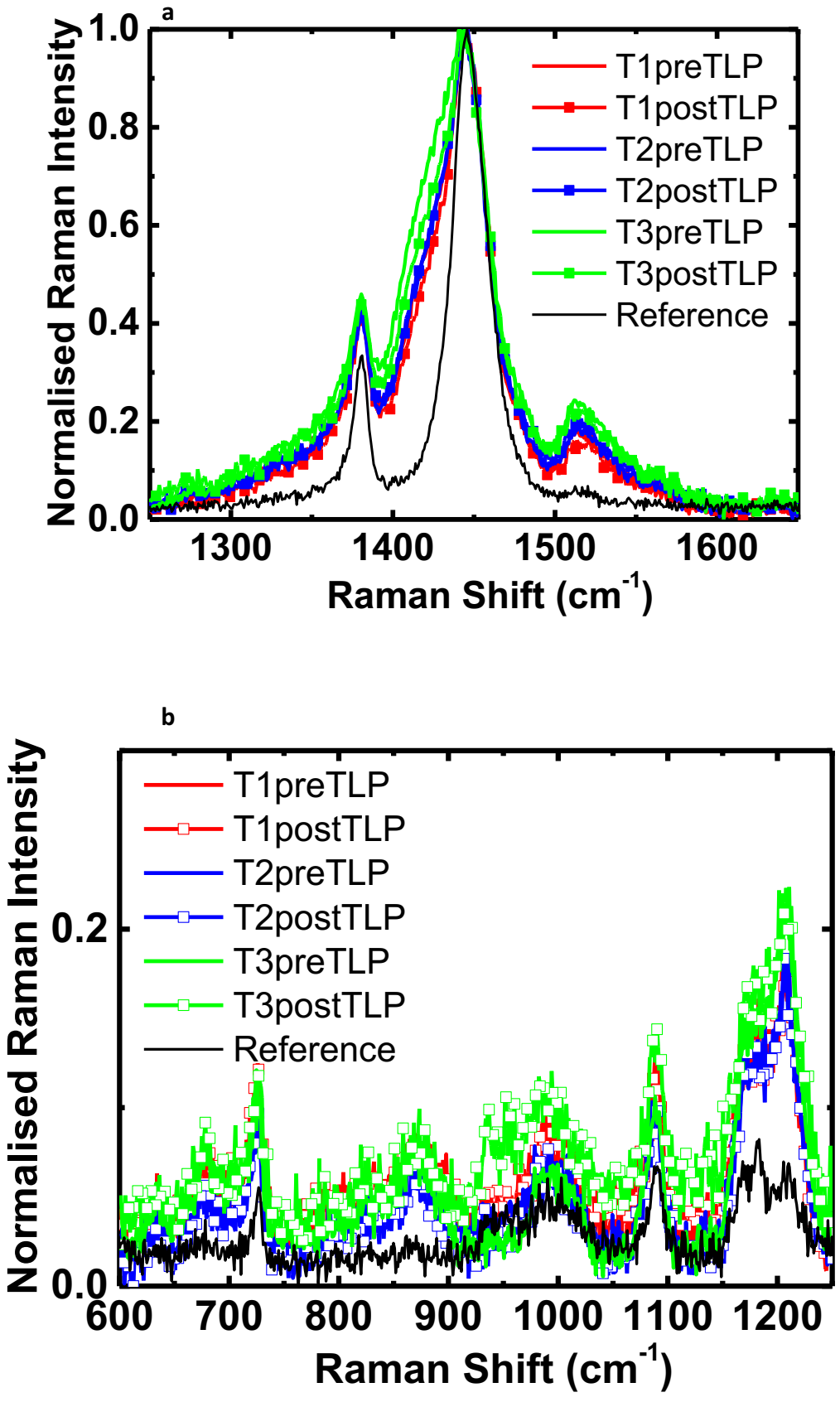


Figure 4-5: The normalised Raman spectra, within the range 600-1250 cm^{-1} (a), and 1250-1700 cm^{-1} (b) of P3HT OFETs that have undergone neutrons aging according three different doses (T1=4 hrs, T2=12 hrs, T3=24 hrs) and DSpos TLP stress test.

The portion 1250-1700 cm^{-1} is characterised by the symmetric stretch of the C=C in-plane ring mode at 1445 cm^{-1} (C_α=C_β stretching), by the C-C intraring stretch mode at 1381 cm^{-1} (C_β-$C_{\beta'}$ stretching) and by the C=C anti-symmetric stretch at 1515 cm^{-1} ($C_{\alpha'}$=$C_{\beta'}$ stretching) [10], [137], [166]. This region of the P3HT Raman spectrum is sensitive to π-electron delocalisation and structural order degradation. In Figure 4-4a, these three peaks are clearly depicted. The portion 600-1300 cm^{-1} is characterised by a C-C inter-ring stretch mode (C_α-$C_{\alpha'}$ stretching) at 1208 cm^{-1}, by a C-H bending (C_β-H bending) at 1090 cm^{-1} and at 1182 cm^{-1}, by a C-C_{alkyl} stretch mode ($C_{\beta'}$-C_{alkyl} stretching) at 997 cm^{-1}, a C-S-C (C_α-S-$C_{\alpha'}$) deformation mode at 724 $cm^{-1}$and at 683 cm^{-1}. These peaks can be appreciated in Figure 4-5b.

Analysing the portion 1250-1700 cm^{-1} first, a remarkable broadening of 1445 cm^{1} peak is reported in all the spectra represented. The portion of the spectra between the peaks at 1445 cm^{-1} and 1381 cm^{-1} is characterised by a low-energy wing of the C=C symmetric stretching localised at the 1430 cm^{-1}. This phenomenon is reported in literature as consequent to the transition from an ordered to a disordered molecular organisation, usually due to the oxidation of the P3HT chains, and resulting in a quinoid form of the P3HT[10], [137]. Oxidation can affect these devices independently of neutrons irradiation. However, Raman spectra collected from pristine devices, built during the same fabrication session of the tested-ones, stored the same interval of time in analogous conditions of the tested-ones and analysed at the Raman spectroscope within the same session of the others, do not show such low-energy wing, therefore I assume that neutrons irradiation forced polymer chains to a quinoid form, worsening their molecular organisation. Such oxidation of the polymer happens regardless of the TLP tests. The 1381 cm^{-1} spectra appear broader and enhanced in comparison with the spectrum of the pristine sample. Such variation is expectably due to a general increase of the disorder of P3HT polymer chains induced by a reduction of the conjugation length of the poly(thiophene) films, a factor also causing the broadening observed in the other peaks of this portion of the spectra. The 1515 cm^{-1} peaks strong enhancement is most probably due to the formation of no-coplanar segments of the chains inducing a torsional disorder to polymer chains. The formation of these no-coplanar segments is also responsible for the enhancement that can be observed in the 1210 cm^{-1} and 728 cm^{-1} peaks. Looking at rest of the portion 600-1250 cm^{-1}, the peaks at 683 cm^{-1} appear enhanced because of the C-S-C deformation, also responsible for the enhancement of the 728 cm^{-1} peaks. The induced torsional stress on P3HT chains justifies the enhancement observed in the 997 cm^{-1} peaks, due to the stretch of the C-C_{alkyl}. Such peaks are particularly broader for samples DSpos stressed that were previously treated

according T3 dose, therefore pointing out a strong C-S-C deformation in such samples. The enhancement of the peaks at 1182 cm^{-1} and at 870 cm^{-1} are both connected to a weakening of P3HT stability, consequently to a strong alteration of the polymer order, also meaning a de-doping process taking place within the polymer and formation of dication species. These two peaks are markedly broader and greater in the DSpos stressed OFETs previously treated according the T3 dose.

Except for the peak at 997 cm^{-1}, differences between spectra taken from devices treated according the same neutrons irradiation dose and the spectra taken from the same devices after the DSpos TLP treatment are negligible. Interestingly, the spectra show a trend that locates T3 treated OFETs spectra as the most broadened and enlarged, followed by the spectra collected from the T2 and T1 treated devices.

4.1.4 **Discussion**

The degradation of the electric parameters with respect to the sole neutrons irradiation can reasonably be ascribed to the formation of neutron-induced defective species in the channel[187]. Paternò et al. [10] observed that these defective species can be removed by annealing the samples. The formation of no-coplanar segments, and hence of polaronic species, as a matter of facts, is a doping process to the P3HT. However, the reduction of the mobility and of other OFETs figures, more and more evident with the increase of neutrons irradiation dose, shows that the overall degradation that polymer chains suffer because of neutrons overcomes by far the benefits due to the formation of localised states because of induced defects. Furthermore, as seen in the Raman spectra, P3HT molecular stability is dramatically decreased and de-doping and consequent formation of dication species take place, rendering neutron-induced doping de facto irrelevant[188]. Neutron-induced damages mostly consist in ionisation by nuclear reactions/collisions or in recoil, resonances or cleavage events. Ionisation events originates from direct neutron-nucleus collisions and involve fast neutrons (> 0.1 MeV). Recoil, resonances and cleavage stem from the interaction of epithermal neutrons with the sample nuclei. Cleavage phenomena occur upon collisions transferring an energy large enough to break the C-C or the C-H bonds (~4 eV). Considering the higher fluence of epithermal neutrons generated within VESUVIO beamline (2×10^{15} neutrons cm^{-2}) than the fluence of fast neutrons (> 0.1 MeV) (7.8×10^{8} cm^{-2}), recoil, resonances and cleavage are more likely to happen than ionisation. Interaction with epithermal neutrons can take place via either scattering or absorption. In fact, conjugated polymers,

and organic matter in general, are significantly rich in hydrogen atoms, therefore neutron scattering intensively interests such materials[189].

The results obtained from DSpos tests of neutrons hardened OFETs are clearly affected by the dose of neutrons irradiation they were exposed to before the DSpos treatment. A great displacement of both TLP parameters and electrical parameters values occurs between samples treated according T1 and samples treated according T2, but between T2 and T3 the degradation looks like reaching a sort of plateau phase in which its progression is slowed down. TLP parameters obtained from devices neutrons aged according T1, are similar with those observed for P3HT OFETs tested according the DSpos test described in section 3.2.2.3.1. However, comparing these two cases, the degradation of P3HT molecular order shown by Raman spectra causes a lowering of the charge mobility, and thus, a lowering of the I_{TLP} values necessary to reach the trigger point as well as an increase of R_{TLP} values. Therefore, a slight loss of the TLP figures is caused by the neutrons irradiation in these devices, if compared with P3HT OFETs uniquely TLP stressed. The presence of the snapback underlines that parasitic paths arise within the device and partially release the pulsed energy after the trigger point. Passing from T1 to T2, such TLP figures are dramatically decreased, underlining how neutrons irradiation has significantly reduced these devices resilience to TLP stress. Values are similar between T2 and T3. Such loss is mostly due to the heavy distortions P3HT undergoes after being irradiated according T2 and T3, as shown in Raman spectra. Notably, the R_{TLP} values observed in these devices are the highest observed so far in P3HT OFETs treated with TLP pulses, reaching values as high as 26 kΩ. Such increase can be ascribed to the lowering of the charge mobility T2 and T3 cause in P3HT. The heavy reduction of the on/off ratio, reaching a factor of 10 in T3 treated devices (around 10^4 in pristine devices), is mostly due to the lower value of I_{DSMAX} reached by these devices, rather than an increase of the subthreshold current that was found ranging between 0.5 μA and 0.1 μA regardless of the neutrons dose devices were exposed to. Thus, neutrons irradiation mostly affects the P3HT film of the devices.

4.1.5 Conclusions

I exposed P3HT OFETs to three different doses (aging periods) of neutrons irradiation, namely 4 hrs (T1), 12 hrs (T2) and 24 hrs (T3), by taking advantage of VESUVIO beamline within the pulsed neutron source ISIS, RAL labs in the Oxfordshire. Such doses, according the energy spectrum of neutrons generated in the VESUVIO beamline, are equivalent to the exposure equipment undergo on ISS for 40, 120 and 240 years, respectively. I subsequently treated these devices by applying

positive pulses between the drain and the source, keeping the gate grounded (DSpos). T1 dose was found to decrease electrical parameters of transistors, especially the mobility, which suffers of a tenfold reduction. Furthermore, T1 dose also lowers the resiliency to TLP stress of P3HT OFETs. Both TLP parameters and electrical parameters were found to dramatically decrease passing from T1 to T2, whilst only a small further reduction takes place between T2 and T3. An explanation stems from Raman spectra that show how P3HT suffers of a progressive structural order reduction with the increase of the dose. In particular, a strong C-S-C distortion is pointed out in T3 treated doses. Furthermore, given the nature of the fluence generated within the VESUVIO beamline, which is mostly characterised by epithermal neutrons, collisions, resonances and cleavage are caused by the scattering of such neutrons with highly hydrogenated active layer of OFETs.

Devices treated according T1 were showing an acceptable level of resiliency to TLP stress. Their electrical features, as shown in other studies[10], can be recovered by means of a thermal annealing. Therefore, these devices, provided of ESD protections designed as specified in 3.2.2.5, can be used for spacecraft and aerospace purposes for several years without dramatically compromising their functionality.

4.2 The aging effect on P3HT:PCBM solar cells

In this section, we report on the result we obtained by monitoring the effects of neutrons irradiation on P3HT:PCBM BHJ solar cells neutrons hardened for a period of 8 hrs. Throughout the neutrons hardening period, solar cells were exposed to a lamp (tungsten halogen LS-1-CAL Ocean Optics) providing a light intensity of 0.8 Sun (800 W/m^2). Every 15 minutes, JV curves and photovoltaics parameters of exposed cells were measured. In this way, a continuous monitoring of neutrons-induced degradation of OPVs in-operando conditions was obtained. Solar cells were fabricated according the procedure described in 2.2 and characterised as described in 2.2.1. The results here reported were obtained out of three samples. The graphs displayed are representative of all devices.

According the energy spectrum of neutrons generated within the VESUVIO beamline (2.7), the quantity of neutrons characterised by an energy of 10 MeV irradiating a sample in 6 minutes is equivalent to the same number of neutrons with same energy irradiating ISS in 1 year. Therefore, an exposure of 8 hrs is equivalent to an exposure of 80 years on ISS.

At the best of my knowledge, no works are reported about neutrons hardening of organic solar cells in operando conditions.

4.2.1 Neutron aging in operando conditions

In Table 25 are reported the photovoltaics parameters, i.e. the short-circuit current density (J_{SC}), the open-circuit voltage (V_{oc}), the fill factor (FF) and the power conversion efficiency (η), measured before and after exposure to neutrons irradiations for a period of 8 hrs. JV curves of one of the sample measured before and after the neutrons irradiation are reported in Figure 4-6. Both the parameters reported in Table 25 and the curves reported in Figure 4-6 were measured at UCL, therefore by using an impinging light of 1 Sun (1000 W/m^2). On the contrary, curves displayed in Figure 4-7 and Figure 4-8 were measured during the neutrons soaking by means of a 0.8 Sun source light.

Table 25: Photovoltaics parameters of P3HT:PCBM OPVs before and after the exposure to neutrons irradiation for 8 hrs.

	J_{sc} (mA/cm^2)	V_{oc} (V)	FF	η (%)
Sample 1-pre n.h.	8.4	0.57	0.49	2.37
Sample 1-post n.h.	7.87	0.54	0.44	1.86
Sample 2-pre n.h.	8.65	0.59	0.51	2.57
Sample 2-pre n.h.	8.11	0.54	0.45	2.01
Sample 3-pre n.h.	8.35	0.58	0.49	2.51
Sample 3-pre n.h.	7.5	0.54	0.44	1.94
Mean variation (%) pre-after n.h.	-6.67%	-7.03%	-10%	-22.13%

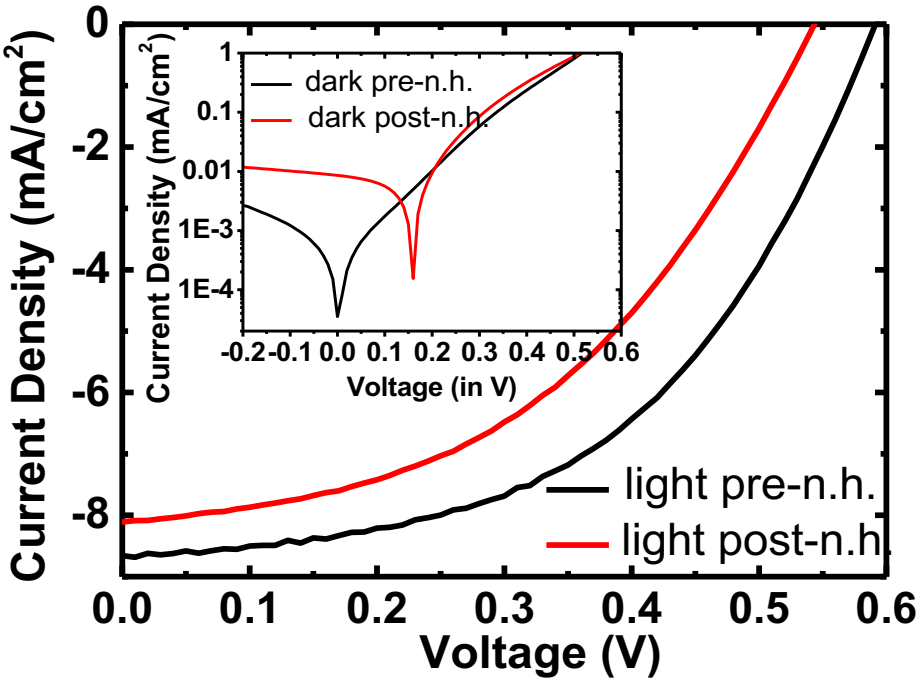


Figure 4-6: JV curves of a P3HT:PCBM sample before and after 8 hrs of neutron hardening (n.h.) exposure.

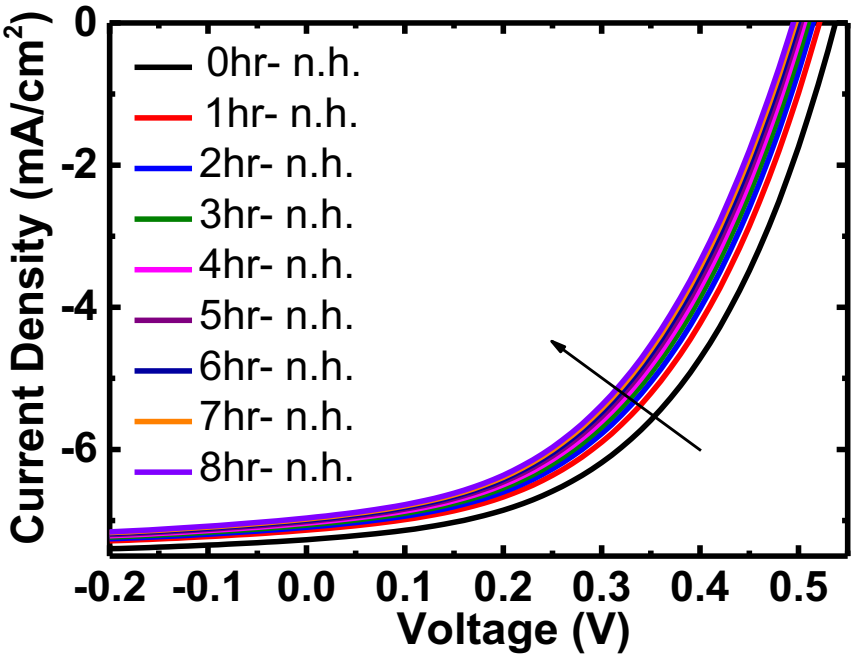


Figure 4-7: JV curves of neutrons irradiated P3HT:PCBM OPVs measured during the neutrons soaking by means of a 0.8 Sun light source. Curves reported in the graph were measured after each hour of exposure.

Neutrons irradiation causes a reduction, on average, by 6.67%, by 7.03%, by 10% and by 22.13% of the pristine J_{SC}, V_{oc}, FF and η respectively (Table 25). The current dark is increased by almost two orders of magnitude after the exposure to neutrons, as seen in the inset of Figure 4-6. Looking at the graphs related to the in-operando conditions, we see from Figure 4-7 that curves measured from the same sample after each hour of exposure are progressively reaching lower values of J_{SC} and V_{oc}. The decrease of these two parameters is shown in Figure 4-8a, and consequently, also the FF and the η are reduced, as shown in Figure 4-8b, since the last two directly depend from the first two according the equations 1.3 and 1.4. However, FF and η also depend from the J_{Pmax} and the V_{Pmax}, but these are also reduced since the area of each curve measured after each hour of exposure is progressively lowered. Interestingly, the parameters reduction rate is not linearly dependent with the time of exposure. The largest variation takes place within the first hour of exposure as J_{SC}, V_{oc}, FF and η suffer of a reduction by 1.6%, 2.6%, 1.76% and 5.98%, respectively. In the second hour, the decrease rate slows down and only a further reduction by 0.6%, 1.3%, 1.05% and 2.8% affect respectively the J_{SC}, the V_{oc}, the FF and the η. As hours pass, the decrease rate is progressively lower. In the last hour, the reduction rate interesting the J_{SC}, the V_{oc}, the FF and the η is of 0.2%, 0.43%, 0.34% and 0.9%, respectively. Therefore, irradiated neutrons progressively exhaust sample nuclei response.

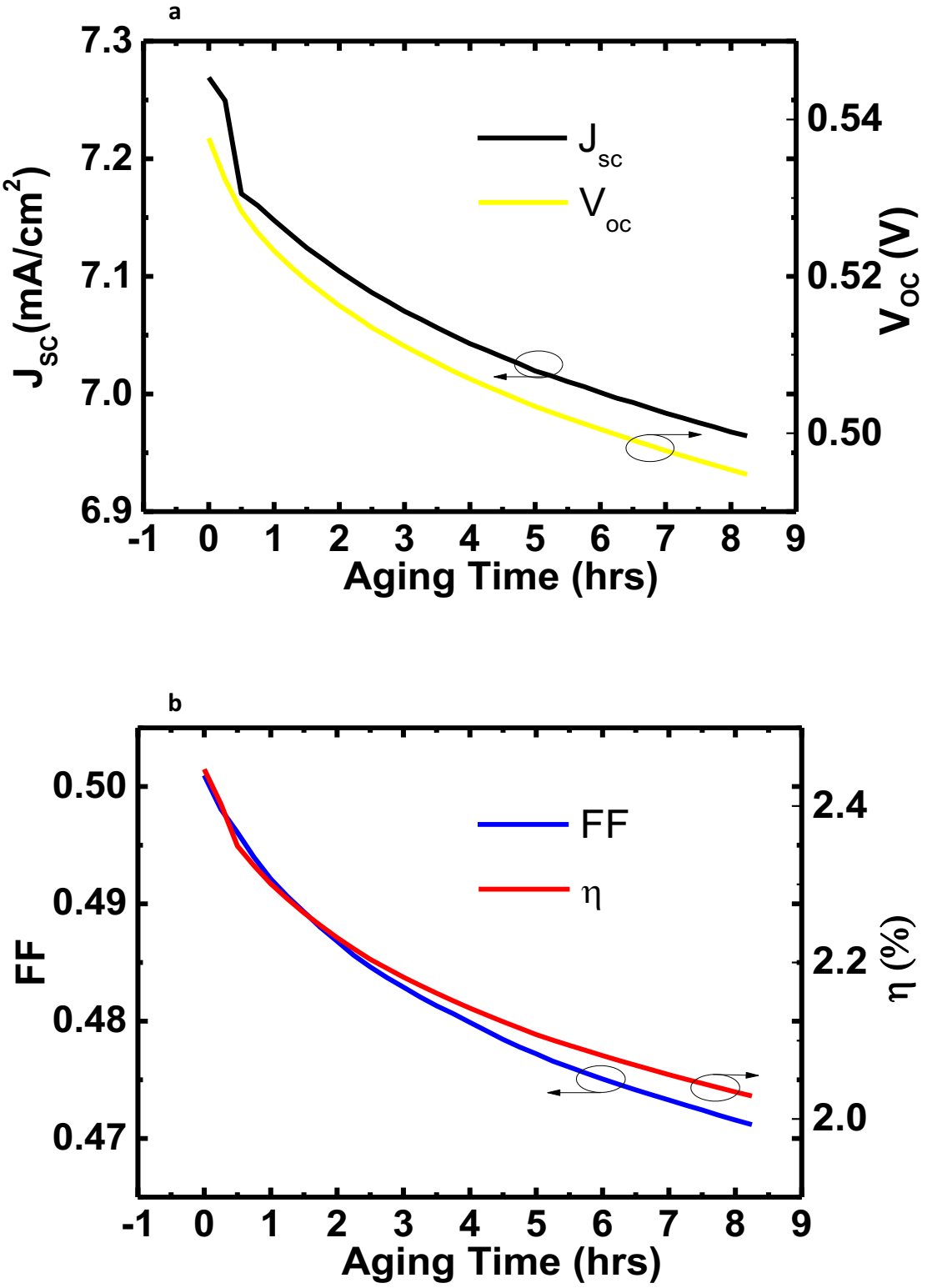


Figure 4-8: the progressive loss of OPVs figures during the neutron soaking. Above (a) are reported the short-circuit current (J_{sc}) and the open-circuit voltage (V_{oc}), whereas below (b) are reported the fill factor (FF) and the power conversion efficiency (η). These values were measured every 15 minutes during the soaking time.

4.2.2 **Discussion**

According to the equivalent circuit model for a solar cell[79], [80] (Figure 1-12), the decrease of FF can be explained as consequent to an increase of the R_s, therefore the resistive paths that charges encounter at the electrodes are increased by the neutrons irradiation. In fact, electrodes can be significantly altered because of fast neutrons (>0.1 MeV) causing cleavage or recoil. The decrease of the V_{oc} is linked with the R_{SH}, which represents the resistance across the active layer. Such resistance is lowered during the neutrons irradiation causing the produced photo-current to be internally dispersed, most probably because of a joint effect of neutron-induced doping of the active layer and ionisation of nuclei, causing the enhancement of charges traps within the same. These phenomena also explain the increase of the dark current. The latter is described by the current I_D, which takes in account the recombination of charges within the device. In dark conditions, for an I_L equal to 0, I_D is favoured by a low R_{SH} and a high R_S. The combination of all these factors lead to the decrease of the η.

As observed in the previous section, the neutrons fluence is characterised by a higher fluence of epithermal neutrons generated within VESUVIO beamline (2×10^{15} neutrons cm^{-2}) than fast neutrons (> 0.1 MeV) (7.8×10^{8} cm^{-2}). This enhances the likelihood of recoil, resonances and cleavage rather than ionisation. Cleavage phenomena occur upon collisions transferring an energy large enough to break the C-C or the C-H bonds (~4 eV).

The photovoltaics reduction rate reducing during the exposure can be explained as a progressive increase of the energy required to force the lattice to accumulate further defects, as time exposure increases[190], [191].

4.2.3 **Conclusions**

I exposed to neutrons irradiation P3HT:PCBM samples according a period of 8 hrs. During such period of exposure, samples receive the same quantity of neutrons they would receive in 80 years on ISS. Samples were exposed to neutrons irradiation while left in operando conditions, i.e. samples were exposed to an impinging light equivalent to 0.8 Sun and their photovoltaics features were constantly monitored throughout the neutrons irradiation. Curves measured during the exposure reveal a progressive reduction of all photovoltaics parameters. Interestingly, such degradation is not linearly dependent with the time of exposure, on the contrary the highest reduction of the photovoltaic performance parameters is concentrated within the first hour of exposure. For instance, the η is reduced of almost the 6% within the first hour but only by 0.9% between the 7^{th}

and the 8th hour. The reason that explains such phenomenon lies in the lattice progressively requiring a higher energy to allow further neutrons-induced defects. In total, the mean reduction by J_{SC}, V_{oc}, FF and η is equal to the 6.67%, by 7.03%, by 10% and by 22.13%, respectively. Such alterations can be ascribed to a joint effect of the decrease of the resistance across the device active layers and to the increase of recombination of charges taking place within the polymer in dark condition. These phenomena are due to neutron-induced doping and enhancement of charge traps because of ionisation. Furthermore, an increase of the resistance of electrodes due to cleavage or recoil is also taking place. Nevertheless, considering the neutron ageing these devices undergo and the relatively low loss of performance found afterwards, P3HT:PCBM OPVs are unexpectedly robust to neutrons irradiation. This finding paves the route towards a massive employment of organic solar cells for spacecraft applications, considering also all the other well-known properties organic semiconductor are characterised of, such as lightweight, easy and cheap manufacturing, flexibility and large-area scalability.

4.3 Chapter Conclusions

In this chapter, I reported on the results I obtained from two experiment involving neutron irradiations. To carry out these experiments, I took advantage of VESUVIO beamline within the pulsed neutron source ISIS, RAL labs in the Oxfordshire. The energy spectrum of the generated neutron within this source is characterised by a higher fluence of epithermal neutrons (2×10^{15} neutrons cm^{-2}) than fast neutrons (> 0.1 MeV) (7.8×10^{8} cm^{-2}). This enhances the likelihood of recoil, resonances and cleavage rather than ionisation in samples treated accordingly. Furthermore, the quantity of neutrons characterised by an energy of 10 MeV reaching a sample within this beamline in 6 minutes is equivalent to the quantity of neutrons of the same kind reaching ISS in 1 year.

In the first experiment, I exposed P3HT OFETs to three different doses (aging period) of neutrons irradiation, namely 4 hrs (T1), 12 hrs (T2) and 24 hrs (T3). T1 dose was found to decrease electrical parameters of transistors, especially the mobility that suffers a tenfold reduction, and to lower resiliency to TLP stress of P3HT OFETs. Both TLP parameters and electrical parameters were found to dramatically decrease passing from T1 to T2, whilst a further reduction takes place between T2 and T3. Raman spectra show P3HT suffers of a progressive structural order reduction with the increase of the dose. In particular, a strong C-S-C distortion is pointed out in T3 treated doses.

Devices treated according T1 were showing an acceptable level of resiliency to TLP stress. Their electrical features can be recovered by means of a thermal annealing. Provided of ESD protections, designed as specified in 3.2.2.5, these devices can be used for spacecraft and aerospace purposes for several years without compromising their functionality.

In the second experiment, I exposed to neutrons irradiation P3HT:PCBM samples according a period of 8 hrs. Samples were exposed to neutron irradiation while left in operando conditions, i.e. samples were exposed to an impinging light equivalent to 0.8 Sun and their photovoltaics features were constantly monitored throughout the neutrons irradiation. Curves measured during the exposure reveal a progressive reduction of all photovoltaics performance parameters. Such degradation is not linearly dependent with the time of exposure since the lattice progressively requires a higher energy to allow further neutrons-induced defects. In total, J_{SC}, V_{oc}, FF and η are reduced by 6.67%, by 7.03%, by 10% and by 22.13%, respectively. Such alterations can be ascribed to a joint effect of the decrease of the resistance across the device active layers and to the increase of recombination of charges taking place within the polymer in dark condition. These phenomena are due to neutron-induced doping and enhancement of charge traps because of ionisation. Furthermore, an increase of the resistance of electrodes due to cleavage or recoil also takes place. Seen the neutron aging these devices undergo and the relatively low loss of figures, P3HT:PCBM OPVs are extraordinary robust to neutrons irradiation. A massive employment of organic solar cells for spacecraft applications, considering also all the other well-known properties organic semiconductors are characterised of, such as lightweight, easy and cheap manufacturing, flexibility and large-area scalability, is reasonably to occur within next few years.

5. Summary and Conclusions

In this thesis, I aimed at providing some insight on the characterisation of the response of organic devices to the environmental stress that affect equipment used in application fields such as medicine, robotics, avionics, i.e. to electrostatic discharge and neutrons irradiation. In particular, I chose P3HT and PBTTT OFETs, F8BT OLEDs and P3HT:PCBM OPVs and I furnished new perspectives for the employment of these devices on a large scale. ESD phenomena were obtained by means of a TLP system provided by the ATIS group at Fraunhofer research institution for microsystems and solid state technologies (EMFT), whereas neutrons irradiation was obtained by means of the VESUVIO beamline within the ISIS muon and neutron pulsed source. The results regarding the TLP characterisation were obtained thanks to a collaboration carried out with Dr. H. Gieser and Dr. Lim from the ATIS group, with whom I published part of the results in this thesis reported. The results regarding the neutrons irradiation were obtained thanks to a collaboration with Dr. Paternò and Dr. Garcia Sakai. In this chapter, I summarise the findings illustrated in this thesis work and I give few insights into future work.

In chapter 3, I characterised the response to TLP stress of three different organic devices, namely OPVs, OLEDs and OFETs. I tested P3HT:PCBM OPVs according positive and negative pulses. OPVs tested by means of positive pulses withstand currents higher than 3 A, dissipating an incoming power higher than 800 W without incurring into permanent damages. Furthermore, the photovoltaic parameters of such devices result improved with a final η increased of roughly 14% respect to the pristine ones. On the other hand, the same devices resulted much weaker in the case of negative applied pulses. OPVs can act as ESD protections due to the low values of R_{TLP} these devices feature. Protections for P3HT:PCBM OPV need to avoid that pulsed energy, I_{TLP} and V_{TLP} higher than 0.32 μJ, 0.13 A and 29 V, respectively, reach the device.

In this same chapter, I characterised the response to TLP tests of P3HT and PBTTT OFETs according six different TLP conditions obtained by combining three different applied bias to the gate of such devices, namely 0 V, 10 V and -20 V, and by applying both positive and negative drain-source pulses per each of these gate biases. Furthermore, I characterised the response to TLP pulses applied between the drain and the gate of the OFETs leaving the source unconnected and by using both positive and negative pulses. The electrostatic discharges are particularly destructive whenever

these involve the silicon oxide of the devices, pointing out the necessity to adopt ESD protections. Tests involving the drain and the source resulted particularly damaging for the interdigitated metal contacts regardless of the applied gate bias. A snapback region in the I_{TLP}-V_{TLP} curves of both P3HT and PBTTT OFETs were observed. The negative applied pulses, regardless of the applied bias on the gate, do not completely compromise the functionality of the devices. However, the mobility, the threshold and the on/off ratio of these devices result particularly affected. Raman spectra collected from all the TLP tested OFETs show a higher resiliency of PBTTT OFETs to the TLP stress presumably thanks to its significantly more crystalline structure. Both P3HT and PBTTT OFETs feature R_{TLP} values close or higher than 1 kΩ, too high to suggest these devices as ESD protections. Instead, ESD protections need to be designed for these devices. Protections between drain and source require to comply with these criteria: maximum allowed E_{TLP} = 0.65 μJ; maximum allowed I_{TLP} = 0.037 A; maximum V_{TLP} = 102 V. Protections are also required between the gate and the drain/source: maximum E_{TLP} = 3.4 μJ; maximum I_{TLP} = 0.2 A; maximum V_{TLP} = 168 V.

In the third part of chapter 3, I tested F8BT OLEDs in three different operating conditions, i.e. when no bias is applied between the anode and the cathode and when the OLEDs are on according a bias of 8 V and of 15 V. F8BT OLEDs tested with positive pulses and with no applied bias maintained their functionality. However, I found TLP tests increasing the V_{on} of almost 0.5 V and altering the JV curves of these OLEDs, also causing red-shift of the EL curves. TLP was found to enhance the conductivity of the active layer of devices while at the same time disrupting their rectifying behaviour. Such process is more evident in devices biased and tested with negative pulses. Nonetheless, the TLP parameters found for F8BT OLEDs reveal unexpected robustness to ESD events of these devices that, due to low value of R_{TLP}, can also be used as ESD protections.

In future, the TLP characterisation reported in this thesis can be expanded over organic devices based on different materials, such as perovskites for OPVs, pentacene or indacenodithiophene (IDT) polymers for OFETs and aggregation-induced emission-based (AIE) polymers for OLEDs[192]–[194]. Furthermore, Raman spectroscopy on OPVs and OLEDs would shed light on the status of materials after the exposure to TLP stress, although this means to avoid adopting encapsulated devices and dealing with more fragile samples. X-ray photoelectron spectroscopy (XPS) could help in understanding if molecules from other layers migrate into the active layers of OPVs and OLEDs upon TLP applied pulses. Moreover, PL efficiency and time-correlated single-photon counting (TCSPC) would help in investigating the effect of the TLP stress on the excitons forming process within OLEDs.

In chapter 4, I reported the results I obtained from two experiment involving neutron irradiations. The energy spectrum of the generated neutron within this source is characterised by a higher fluence of epithermal neutrons (2×10^{15} neutrons cm^{-2}) than fast neutrons (> 0.1 MeV) (7.8×10^{8} cm^{-2}). This enhances the likelihood of recoil, resonances and cleavage rather than ionisation in samples treated accordingly. Furthermore, the quantity of neutrons characterised by an energy of 10 MeV reaching a sample within this beamline in 6 minutes is equivalent to the quantity of neutrons of the same kind reaching ISS in 1 year.

In the first experiment, I exposed P3HT OFETs to three different doses (aging periods) of neutrons irradiation, namely 4 hrs (T1), 12 hrs (T2) and 24 hrs (T3). I subsequently treated these devices by applying positive pulses between the drain and the source, keeping the gate grounded. T1 dose was found to decrease electrical parameters of transistors and to lower resiliency to TLP stress of P3HT OFETs. Both TLP parameters and electrical parameters were found to dramatically decrease passing from T1 to T2. Raman spectra show that P3HT suffers of a progressive structural order reduction with the increase of the dose. Nevertheless, devices treated according T1 were showing an acceptable level of resiliency to TLP stress. Provided of ESD protections designed as specified in chapter 4, these devices can be used for spacecraft and aerospace purposes over considerable long period of time without dramatically compromise their operation and functionality.

In the second experiment, I exposed to neutron irradiations P3HT:PCBM OPVs samples according a period of 8 hrs, and in operando conditions, i.e. while exposed to an impinging light equivalent to 0.8 Sun. The photovoltaics features of these devices were constantly monitored throughout the neutrons irradiation. Curves measured during the exposure reveal a progressive reduction of all photovoltaics parameters. Such degradation is not linearly dependent with the time of exposure, since the lattice progressively requires a higher energy to allow further neutrons-induced defects. In total, the reduction of the J_{SC}, V_{oc}, FF and η is by 6.67%, by 7.03%, by 10% and by 22.13%, respectively. Such alterations can be justified as a synergistic effect of the decrease of the resistance across the device active layers and of the increase of recombination of charges taking place within the polymer in dark condition. These phenomena are caused by neutron-induced doping and enhancement of the concentration of charge traps because of ionisation. Furthermore, an increase of the resistance of electrodes due to cleavage or recoil is also taking place. The relatively low degradation of figures points out that P3HT:PCBM OPVs are extraordinary robust to neutrons irradiation if compared to silicon-based optoelectronics, which upon exposure to neutrons in space suffer of a tenfold decrease of figures of merit and remain significantly radioactive for long

periods[24], [195]. A massive employment of organic solar cells for spacecraft applications, considering also the lightweight, the easy and cheap manufacturing, the flexibility and the large-area scalability organic semiconductors can provide, reasonably is expected to take place within next few years.

In future, the neutron aging tests can be repeated on OLEDs as well as on OPVs and OFETs based on other materials, such as perovskites or pentacene. Furthermore, X-ray, PL and Raman spectroscopy can be carried out on neutron aged organic devices to get insights into material alterations induced by the exposure to neutrons.

Interestingly, the results in this thesis reported show how polymer-based devices are robust to both ESD and cosmic ray stress. Silicon-based technology is found to suffer a permanent failure in most of the cases for an applied TLP power lower than 400 W [15], [23], whilst polymer based technology was found to withstand up to 800 W (OPVs and OLEDs) without suffering permanent damages. As regards the stress correlated to the exposure to a similar dose of neutron irradiation, optoelectronic devices based on inorganic semiconductors suffer of a tenfold increase of the dark current causing the figures of merit correlated (J_{SC}, η) to be reduced up to the ~90% of their pristine values [24], whilst the same figures in polymer-based devices suffer a reduction of ~20% only.

Although previous works are reported in literature, the work reported in this thesis, at the best of my knowledge, is the first work reporting a systematic quantitative TLP characterisation of organic devices along with a qualitative description of the effects on the organic materials within these devices because of the conditions imposed by the TLP test: i) high-frequency; ii) high-voltage. As observed in the experiments in this thesis reported regarding the OPVs and the OLEDs, in which metal lines are big enough to sustain very high current without damaging, whenever similar conditions apply, the TLP can be used as a tool to directly assess the behaviour of organic semiconductors in a high frequency domain. In fact, because of their slow reaction, organic materials have been poorly explored within high frequency domains but the results highlighted in this thesis opens new scenario to such materials. Furthermore, under same conditions (robust metal connections between the instrument-the device pads-the device metal lines) also the response to high-voltage conditions can be explored, assessing if cracks open within the films, to measure the resistance of polymers in correspondence of both i and ii, to gain insights into effects of mobility on the capability of materials in discharge the pulsed energy, or to study how external applied bias affect polymers response. On the other hand, whenever the robust metal connections between the

instrument-the device pads-the device metal lines conditions cannot be satisfied, as observed in the OFETs tested into these thesis, the TLP can be used as a tool to investigate failure dynamics and how external bias can alter this one diverting the failure in different points of the DUT. Therefore, this thesis opens a new scenario proposing an investigating tool aimed both at measuring parameters useful for the design of the devices and at highlighting organic materials properties that can lead organic electronics to gain its definitive momentum.

Bibliography

[1] C. K. Chiang, C. R. J. Fincher, Y. W. Park, A. J. Heeger, H. Shirakawa, E. J. Louis, S. C. Gau, and A. G. Macdiarmid, "Electrical Conductivity in Doped Polyacetylene," *Phys. Rev. Lett.*, vol. 39, no. 17, pp. 1098–1101, 1977.

[2] H. Shirakawa, E. J. Louis, A. G. MacDiarmid, C. K. Chiang, and A. J. Heeger, "Synthesis of electrically conducting organic polymers: halogen derivatives of polyacetylene, (CH)," *J. Chem. Soc. Chem. Commun.*, no. 16, pp. 578–580, 1977.

[3] S. Logothetidis, "Flexible organic electronic devices : Materials , process and applications," *Mater. Sci. Eng. B*, vol. 152, pp. 96–104, 2008.

[4] Y. Sun and J. A. Rogers, "Inorganic Semiconductors for Flexible Electronics," *Adv. Mater.*, vol. 19, pp. 1897–1916, 2007.

[5] F. Cacialli, "Organic semiconductors for the new millennium," *Philos. Trans. R. Soc. London A Math. Phys. Eng. Sci.*, vol. 358, no. 1765, pp. 173–192, 2000.

[6] J. A. Rogers and Y. Huang, "A curvy, stretchy future for electronics.," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 106, no. 27, pp. 10875–6, Jul. 2009.

[7] D. M. de Leeuw and E. Cantatore, "Organic electronics: Materials, technology and circuit design developments enabling new applications," *Mater. Sci. Semicond. Process.*, vol. 11, no. 5, pp. 199–204, 2008.

[8] V. Robbiano, A. Abdellah, L. Santarelli, A. Falco, S. El-molla, L. V Titova, D. N. Purschke, F. A. Hegmann, F. Cacialli, and P. Lugli, "Analysis of Sprayed Carbon Nanotube Films on Rigid and Flexible Substrates," in *Nanotechnology (IEEE-NANO), 2014 IEEE 14th International Conference on.*, 2014, pp. 650–654.

[9] H. Kawaguchi, T. Someya, T. Sekitani, and T. Sakurai, "Cut-and-paste customization of organic FET integrated circuit and its application to electronic artificial skin," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 177–185, 2005.

[10] G. M. Paternò, V. Robbiano, K. J. Fraser, C. Frost, V. García Sakai, and F. Cacialli, "Neutron Radiation Tolerance of Two Benchmark Thiophene-Based Conjugated Polymers: the Importance of Crystallinity for Organic Avionics," *Sci. Rep.*, vol. 7, p. 41013, Jan. 2017.

[11] D. Kim, J. Ahn, W. M. Choi, H.-S. Kim, T.-H. Kim, J. Song, Y. Y. Huang, Z. Liu, C. Lu, and J. A. Rogers, "Stretchable and Foldable Silicon Integrated Circuits," *Science (80-.).*, vol. 320, pp. 507–511, 2008.

[12] D. J. Lipomi and Z. Bao, "Stretchable, elastic materials and devices for solar energy conversion," *Energy Environ. Sci.*, vol. 4, no. 9, p. 3314, 2011.

[13] G. H. Büscher, R. Kõiva, C. Schürmann, R. Haschke, and H. J. Ritter, "Flexible and stretchable fabric-based tactile sensor," *Rob. Auton. Syst.*, vol. 63, pp. 244–252, 2015.

[14] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *EOS/ESD symposium , vol. 7*, 1985.

[15] A. Amerasekera, L. van Roozendaal, J. Bruines, and F. Kuper, "Characterization and modeling of second breakdown in NMOST's for the extraction of ESD-related process and design parameters," *IEEE Trans. Electron Devices*, vol. 38, no. 9, pp. 2161–2168, 1991.

[16] C. Diaz, S.-M. Kang, C. Duvvury, and L. Wagner, "Electrical overstress (EOS) power profiles: A guideline to qualify EOS of semiconductor devices hardness," *J. Electrostat.*, vol. 31, pp. 161–176, 1993.

[17] J. B. Bates, R. W. Hendricks, and L. B. Shaffer, "Neutron irradiation effects and structure of

noncrystalline SiO2," *J. Chem. Phys.*, vol. 61, no. 10, pp. 4163–4176, Nov. 1974.
[18] A. L. Hopkins, "A Fault-Tolerant Information Processing Concept for Space Vehicles," *IEEE Trans. Comput.*, vol. C-20, no. 11, pp. 1394–1403, Nov. 1971.
[19] T. K. Gaisser, T. Stanev, and S. Tilav, "Cosmic Ray Energy Spectrum from Measurements of Air Showers," *Front. Phys.*, vol. 8, no. 6, pp. 748–758, Mar. 2013.
[20] P. Pareige, R. E. Stoller, K. F. Russell, and M. K. Miller, "Atom probe characterization of the microstructure of nuclear pressure vessel surveillance materials after neutron irradiation and after annealing treatments," *J. Nucl. Mater.*, vol. 249, no. 2–3, pp. 165–174, Oct. 1997.
[21] J. K. Shultis and R. E. Faw, *Radiation shielding*. American Nuclear Society, 2000.
[22] G. Paternò, A. J. Warren, J. Spencer, G. Evans, V. G. Sakai, J. Blumberger, and F. Cacialli, "Micro-focused X-ray diffraction characterization of high-quality [6,6]-phenyl-C61-butyric acid methyl ester single crystals without solvent impurities," *J. Mater. Chem. C*, vol. 1, no. 36, p. 5619, 2013.
[23] V. A. Vashchenko, A. Gallerano, and A. Shibkov, "On chip ESD protection of 600V voltage node," *Proc. Int. Symp. Power Semicond. Devices ICs*, pp. 128–131, 2011.
[24] A. D. Topper, M. J. Campola, D. Chen, M. C. Casey, K.-Y. Yau, D. J. Cochran, K. A. Label, R. L. Ladbury, T. K. Mondy, M. V. O'Bryan, J. A. Pellish, E. P. Wilcox, E. Wyrwas, and M. A. Xapsos, "Compendium of Current Total Ionizing Dose and Displacement Damage Results from NASA Goddard Space Flight Center and NASA Electronic Parts and Packaging Program," Jul. 2017.
[25] C. Kiparissides, "Polymerization reactor modeling: A review of recent developments and future directions," *Chem. Eng. Sci.*, vol. 51, no. 10, pp. 1637–1659, May 1996.
[26] F. Di Stasio, L. Berti, S. O. McDonnell, V. Robbiano, H. L. Anderson, D. Comoretto, and F. Cacialli, "Fluorescent polystyrene photonic crystals self-assembled with water-soluble conjugated polyrotaxanes," *APL Mater.*, vol. 1, no. 4, 2013.
[27] J. J. Michels, M. J. O'Connell, P. N. Taylor, J. S. Wilson, F. Cacialli, and H. L. Anderson, "Synthesis of Conjugated Polyrotaxanes," *Chem. - A Eur. J.*, vol. 9, no. 24, pp. 6167–6176, 2003.
[28] B. S. Mitchell, *An Introduction To Materials Engineering and Science: for Chemical and Materials Engineers*. WILEY-INTERSCIENCE, 2004.
[29] J. A. Brydson, *Plastics materials*, 7th Editio. Elsevier, 1995.
[30] P. J. Flory, *Principles of Polymer Chemistry*. New York: Cornell University Press, 1953.
[31] M. Angelopoulos, "Conducting polymers in microelectronics," *IBM J. Res. Dev.*, vol. 45, no. 1, pp. 57–75, 2001.
[32] H. Sirringhaus, N. Tessler, and R. H. Friend, "Integrated optoelectronic devices based on conjugated polymers," *Sci. (80-.).*, vol. 280, no. 5370, pp. 1741–1744, 1998.
[33] S. Savagatrup, A. S. Makaram, D. J. Burke, and D. J. Lipomi, "Mechanical Properties of Conjugated Polymers and Polymer-Fullerene Composites as a Function of Molecular Structure," *Adv. Funct. Mater.*, vol. 24, pp. 1169–1181, 2014.
[34] T. W. Kelley, P. F. Baude, C. Gerlach, D. E. Ender, D. Muyres, M. A. Haase, D. E. Vogel, and S. D. Theiss, "Recent progress in organic electronics: Materials, devices, and processes," *Chem. Mater.*, vol. 16, no. 23, pp. 4413–4422, 2004.
[35] Y.-M. Chien, F. Lefevre, I. Shih, and R. Izquierdo, "A solution processed top emission OLED with transparent carbon nanotube electrodes.," *Nanotechnology*, vol. 21, no. 13, p. 134020, 2010.
[36] S. Ju, J. Li, J. Liu, P.-C. Chen, Y.-G. Ha, F. Ishikawa, H. Chang, C. Zhou, A. Facchetti, D. B. Janes, and T. J. Marks, "Transparent active matrix organic light-emitting diode displays driven by nanowire transistor circuitry.," *Nano Lett.*, vol. 8, no. 4, pp. 997–1004, Apr. 2008.
[37] O. Fenwick, J. K. Sprafke, J. Binas, D. V Kondratuk, D. Stasio, H. L. Anderson, and F. Cacialli,

"Supporting information for : Linear and cyclic porphyrin hexamers as near infra-red emitters in organic light-emitting diodes," *Source*, pp. 8–10, 2011.
[38] T. M. Brown and F. Cacialli, "Contact optimization in polymer light-emitting diodes," *J. Polym. Sci. Part B Polym. Phys.*, vol. 41, no. 21, pp. 2649–2664, 2003.
[39] S. S. Van Bavel, M. Bärenklau, G. De With, H. Hoppe, and J. Loos, "P3HT/PCBM bulk heterojunction solar cells: Impact of blend composition and 3D morphology on device performance," *Adv. Funct. Mater.*, vol. 20, no. 9, pp. 1458–1463, 2010.
[40] A. Facchetti, "π-Conjugated polymers for organic electronics and photovoltaic cell applications," *Chem. Mater.*, vol. 23, no. 3, pp. 733–758, 2011.
[41] H. Sirringhaus, M. Bird, and N. Zhao, "Charge Transport Physics of Conjugated Polymer Field-Effect Transistors," *Adv. Mater.*, vol. 22, no. 34, pp. 3893–3898, Sep. 2010.
[42] M. J. Malachowski and J. Zmija, "Organic field-effect transistors," *Opto-Electronics Rev.*, vol. 18, no. 2, pp. 121–136, 2010.
[43] G. M. Paternò, "Nanoscale Characterisation and Neutron Damage Testing of Organic semiconductors," UCL (University College London), 2016.
[44] G. Tregnago, "Photophysics and applications of organic semiconductors," UCL (University College London), 2015.
[45] P. Y. Yu and M. Cardona, *Fundamentals of Semiconductors*, vol. 1, no. 11. 2010.
[46] T. L. Brown, E. H. J. LeMay, B. E. Bursten, C. J. Murphy, and P. M. Woodward, *Chemistry the Central Science*, 14th ed. Prentice Hall.
[47] G. Li, R. Zhu, and Y. Yang, "Polymer solar cells," *Nat. Photonics*, vol. 6, no. 3, pp. 153–161, 2012.
[48] T.-H. Le, Y. Kim, and H. Yoon, "Electrical and Electrochemical Properties of Conducting Polymers," *Polymers (Basel).*, vol. 9, no. 4, p. 150, Apr. 2017.
[49] Z. Shuai, D. Beljonne, R. J. Silbey, and J. L. Brédas, "Singlet and triplet exciton formation rates in conjugated polymer light-emitting diodes," *Phys. Rev. Lett.*, vol. 84, no. 1, pp. 131–134, 2000.
[50] J.-L. Bredas, J. Cornil, and A. J. Heeger, "The exciton binding energy in luminescent conjugated polymers," *Adv. Mater.*, vol. 8, no. 5, pp. 447–452, May 1996.
[51] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveld-Voss, A. J. H. Spiering, R. A. J. Janssen, E. W. Meijer, P. Herwig, and D. M. de Leeuw, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers," *Nature*, vol. 401, no. 6754, pp. 685–688, 1999.
[52] J. Lange and H. Bassler, "Temperature dependence of the hopping mobility in amorphous tetracene," *Phys. status solidi*, vol. 114, no. 2, pp. 561–569, Dec. 1982.
[53] J. Cornil, D. Beljonne, J.-P. Calbert, and J.-L. Bredas, "Interchain Interactions in Organic π-Conjugated Materials: Impact on Electronic Structure, Optical Response, and Charge Transport," *Adv. Mater.*, vol. 13, no. 14, pp. 1053–1067, Jul. 2001.
[54] M. Wohlgenannt, K. Tandon, S. Mazumdar, S. Ramasesha, and Z. V. Vardeny, "Formation cross-sections of singlet and triplet excitons in π-conjugated polymers," *Nature*, vol. 409, no. 6819, pp. 494–497, Jan. 2001.
[55] J. R. Lakowicz, *Principles of Fluorescence Spectroscopy*. Boston, MA: Springer US, 2006.
[56] J. Morgado, F. Cacialli, J. Gruner, N. Greenham, and R. Friend, "Luminescence properties of poly(p-phenylenevinylene): Role of the conversion temperature on the photoluminescence and electroluminescence efficiencies," *J. Appl. Phys.*, vol. 85, no. 3, pp. 1784–1791, 1999.
[57] R. Riehn, R. Stevenson, D. Richards, D. J. Kang, M. Blamire, A. Downes, and F. Cacialli, "Local probing of photocurrent and photoluminescence in a phase-separated conjugated-polymer blend by means of near-field excitation," *Adv. Funct. Mater.*, vol. 16, no. 4, pp. 469–476, 2006.

[58] P. Barta, F. Cacialli, R. H. Friend, and M. Zagorska, “Efficient photo and electroluminescence of regioregular poly(alkylthiophene)s,” *J. Appl. Phys.*, vol. 84, no. 11, pp. 6279–6284, 1998.
[59] T. Sekitani and T. Someya, “Stretchable , Large-area Organic Electronics,” *Adv. Mater.*, vol. 22, pp. 2228–2246, 2010.
[60] T. Someya and T. Sakurai, “Integration of Organic Field-Effect Transistors and Rubbery Pressure Sensors for Artificial Skin Applications,” in *International Electron Devices Meeting*, 1998, pp. 203–206.
[61] F. Spano, A. Dabrowska, B. M. Quandt, L. Boesel, R. M. Rossi, A. Massaro, and A. Lay-Ekuakille, “Flexible touch sensors based on nanocomposites embedding polymeric optical fibers for artificial skin applications,” in *2015 IEEE 15th International Conference on Nanotechnology (IEEE-NANO)*, 2015, pp. 1295–1298.
[62] S. Betti, R. Molino Lova, E. Rovini, G. Acerbi, L. Santarelli, M. Cabiati, S. Del Ry, and F. Cavallo, “Evaluation of an integrated system of wearable physiological sensors for stress monitoring in working environments by using biological markers,” *IEEE Trans. Biomed. Eng.*, pp. 1–1, 2017.
[63] M. Rinieri, L. Santarelli, L. Fabbri, G. Pastucci, E. Rovini, D. Esposito, S. Pancani, C. Maremmani, F. Vannetti, and F. Cavallo, “Preliminary studies for the evaluation of a novel wearable sensor for biomechanical analysis of upper limbs in Parkinson Disease,” *Gait Posture*, vol. 57, p. 38, Sep. 2017.
[64] E. Rovini, L. Santarelli, D. Esposito, C. Maremmani, and F. Cavallo, “DAPHNE : a novel e-Health system for the diagnosis and the treatment of Parkinson ’ s Disease,” in *foritaal*, 2017, no. July.
[65] J. Gao, A. K. Thomas, R. Johnson, H. Guo, and J. K. Grey, “Spatially Resolving Ordered and Disordered Conformers and Photocurrent Generation in Intercalated Conjugated Polymer/Fullerene Blend Solar Cells.,” *Chem. Mater.*, vol. 26, no. 15, pp. 4395–4404, Aug. 2014.
[66] P. Vanlaeke, A. Swinnen, I. Haeldermans, G. Vanhoyland, T. Aernouts, D. Cheyns, C. Deibel, J. D’Haen, P. Heremans, J. Poortmans, and J. V. Manca, “P3HT/PCBM bulk heterojunction solar cells: Relation between morphology and electro-optical characteristics,” *Sol. Energy Mater. Sol. Cells*, vol. 90, no. 14, pp. 2150–2158, Sep. 2006.
[67] Y. Xu, F. Zhang, and X. Feng, “Patterning of conjugated polymers for organic optoelectronic devices,” *Small*, vol. 7, no. 10, pp. 1338–1360, 2011.
[68] N. Seidler, G. M. Lazzerini, G. Li Destri, G. Marletta, and F. Cacialli, “Enhanced crystallinity and film retention of P3HT thin-films for efficient organic solar cells by use of preformed nanofibers in solution,” *J. Mater. Chem. C*, vol. 1, no. 46, p. 7748, 2013.
[69] H. Youn, H. J. Park, and L. J. Guo, “Organic photovoltaic cells: From performance improvement to manufacturing processes,” *Small*, vol. 11, no. 19, pp. 2228–2246, 2015.
[70] V. D. Mihailetchi, L. J. A. Koster, P. W. M. Blom, C. Melzer, B. De Boer, J. K. J. Van Duren, and R. A. J. Janssen, “Compositional dependence of the performance of poly(p-phenylene vinylene):Methanofullerene bulk-heterojunction solar cells,” *Adv. Funct. Mater.*, vol. 15, no. 5, pp. 795–801, 2005.
[71] T. F. Guo, T. C. Wen, G. L’vovich Pakhomov, X. G. Chin, S. H. Liou, P. H. Yeh, and C. H. Yang, “Effects of film treatment on the performance of poly(3-hexylthiophene)/soluble fullerene-based organic solar cells,” *Thin Solid Films*, vol. 516, no. 10, pp. 3138–3142, 2008.
[72] T. J. K. Brenner, Y. Vaynzof, Z. Li, D. Kabra, R. H. Friend, and C. R. McNeill, “White-light bias external quantum efficiency measurements of standard and inverted P3HT : PCBM photovoltaic cells,” *J. Phys. D. Appl. Phys.*, vol. 45, no. 41, p. 415101, Oct. 2012.
[73] C.-F. Lin, M. Zhang, S.-W. Liu, T.-L. Chiu, and J.-H. Lee, “High Photoelectric Conversion

Efficiency of Metal Phthalocyanine/Fullerene Heterojunction Photovoltaic Device," *Int. J. Mol. Sci.*, vol. 12, no. 12, pp. 476–505, Jan. 2011.
[74] M. C. Scharber, D. Mühlbacher, M. Koppe, P. Denk, C. Waldauf, A. J. Heeger, and C. J. Brabec, "Design rules for donors in bulk-heterojunction solar cells - Towards 10 % energy-conversion efficiency," *Adv. Mater.*, vol. 18, no. 6, pp. 789–794, 2006.
[75] S. Ryu, J. H. Noh, N. J. Jeon, Y. C. Kim, W. S. Yang, J. Seo, and S. Il Seok, "Voltage Output of Efficient Perovskite Solar Cells with high Open-Circuit Voltage and Fill Factor," *Energy Environ. Sci.*, vol. 7, pp. 2614–2618, 2014.
[76] N. J. Jeon, J. Lee, J. H. Noh, K. Nazeeruddin, M. Grätzel, S. Il Seok, M. K. Nazeeruddin, M. Grätzel, and S. Il Seok, "Efficient Inorganic–Organic Hybrid Perovskite Solar Cells Based on Pyrene Arylamine Derivatives as Hole-Transporting Materials," *J. Am. Chem. Soc.*, vol. 135, no. 51, pp. 19087–19090, 2013.
[77] A. Zampetti, "Heterostructures and Interfacial Layers for Polymer Solar Cells," Università Degli Studi Di Roma Tor Vergata, 2013.
[78] F. Cacialli, "Plastic and Molecular Electronics," University College London, 2011.
[79] S. Yoo, B. Domercq, and B. Kippelen, "Intensity-dependent equivalent circuit parameters of organic solar cells based on pentacene and C[sub 60]," *J. Appl. Phys.*, vol. 97, no. 10, p. 103706, 2005.
[80] N. Hossain, S. Das, and T. L. Alford, "Equivalent Circuit Modification for Organic Solar Cells," *Circuits Syst.*, vol. 6, no. June, pp. 153–160, 2015.
[81] T. M. Brown, G. M. Lazzerini, L. J. Parrott, V. Bodrozic, L. Burgi, and F. Cacialli, "Time dependence and freezing-in of the electrode oxygen plasma-induced work function enhancement in polymer semiconductor heterostructures," *Org. Electron. physics, Mater. Appl.*, vol. 12, no. 4, pp. 623–633, 2011.
[82] K. Kwak, K. Cho, and S. Kim, "Stable bending performance of flexible organic light-emitting diodes using IZO anodes.," *Sci. Rep.*, vol. 3, p. 2787, 2013.
[83] S. Sakamoto, M. Okumura, Z. Zhao, and Y. Furukawa, "Raman spectral changes of PEDOT-PSS in polymer light-emitting diodes upon operation," *Chem. Phys. Lett.*, vol. 412, no. 4–6, pp. 395–398, 2005.
[84] J. Morgado, N. Barbagallo, A. Charas, M. Matos, L. Alcacer, and F. Cacialli, "Self-assembly surface modified indium-tin oxide anodes for single-layer light-emitting diodes," *J. Phys. D-Appl. Phys.*, vol. 36, no. 5, pp. 434–438, 2003.
[85] L. H. Smith, J. A. E. Wasey, I. D. W. Samuel, and W. L. Barnes, "Light Out-Coupling Efficiencies of Organic Light-Emitting Diode Structures and the Effect of Photoluminescence Quantum Yield," *Adv. Funct. Mater.*, 2005.
[86] D. Hill, "The Optical Outcoupling of Organic Light Emitting Diodes," *Thesis*, no. June, 2008.
[87] S.-I. Park, Y. Xiong, R.-H. Kim, P. Elvikis, M. Meitl, D.-H. Kim, J. Wu, J. Yoon, C.-J. Yu, Z. Liu, Y. Huang, K. Hwang, P. Ferreira, X. Li, K. Choquette, and J. A. Rogers, "Printed assemblies of inorganic light-emitting diodes for deformable and semitransparent displays.," *Science*, vol. 325, no. 5943, pp. 977–81, Aug. 2009.
[88] Y. Loo, T. Someya, K. W. Baldwin, Z. Bao, P. Ho, A. Dodabalapur, H. E. Katz, and J. A. Rogers, "Soft , conformable electrical contacts for organic semiconductors : High-resolution plastic circuits by lamination," in *PNAS*, 2002, vol. 99, no. 16, pp. 10252–10256.
[89] D. Sainova, S. Janietz, U. Asawapirom, L. Romaner, E. Zojer, and N. Koch, "Improving the Stability of Polymer FETs by Introducing Fixed Acceptor Units into the Main Chain: Application to Poly(alkylthiophenes)," *Chem. Mater.*, vol. 19, no. 6, pp. 1472–1481, 2007.
[90] C. Wang, L. H. Jimison, L. Goris, I. McCulloch, M. Heeney, A. Ziegler, and A. Salleo, "Microstructural Origin of High Mobility in High-Performance Poly(thieno-thiophene) Thin-

Film Transistors," *Adv. Mater.*, vol. 22, no. 6, pp. 697–701, Feb. 2010.
[91] X. Zhang, H. Bronstein, A. J. Kronemeijer, J. Smith, Y. Kim, R. J. Kline, L. J. Richter, T. D. Anthopoulos, H. Sirringhaus, K. Song, M. Heeney, W. Zhang, I. Mcculloch, and D. M. Delongchamp, "Molecular origin of high field-effect mobility in an indacenodithiophene–benzothiadiazole copolymer," *Nat. Commun.*, vol. 4, p. 2238, 2013.
[92] G. Horowitz, "Organic Field-Effect Transistors," *Adv. Mater.*, vol. 10, no. 5, pp. 365–377, 1998.
[93] G. Horowitz, R. Hajlaoui, and F. Kouki, "An analytical model for the organic field-effect transistor in the depletion mode. Application to sexithiophene films and single crystals," *Eur. Phys. J. Appl. Phys.*, vol. 1, no. 3, pp. 361–367, Mar. 1998.
[94] H. N. Raval, S. P. Tiwari, R. R. Navan, S. G. Mhaisalkar, and V. R. Rao, "Solution-processed bootstrapped organic inverters based on P3HT with a high-k gate dielectric material," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 484–486, 2009.
[95] X. Wu, Y. Ma, G. Zhang, Y. Chu, J. Du, Y. Zhang, Z. Li, Y. Duan, Z. Fan, and J. Huang, "Thermally Stable, Biocompatible, and Flexible Organic Field-Effect Transistors and Their Application in Temperature Sensing Arrays for Artificial Skin," *Adv. Funct. Mater.*, vol. 25, no. 14, pp. 2138–2146, Apr. 2015.
[96] Y. Xu, C. Liu, D. Khim, and Y.-Y. Noh, "Development of high-performance printed organic field-effect transistors and integrated circuits.," *Phys. Chem. Chem. Phys.*, vol. 17, pp. 26553–26574, 2014.
[97] Z. Bao, a Dodabalapur, and a J. Lovinger, "Soluble and processable regioregular poly(3-hexylthiophene) for thin film field-effect transistor applications with high mobility," *Appl Phys Lett*, vol. 69, no. 26, pp. 4108–4110, 1996.
[98] G. Horowitz, R. Hajlaoui, H. Bouchriha, R. Bourguiga, and M. Hajlaoui, "The Concept of 'Threshold Voltage' in Organic Field-Effect Transistors," *Adv. Mater.*, vol. 10, no. 12, pp. 923–927, Aug. 1998.
[99] M. Egginger, S. Bauer, R. Schwodiauer, H. Neugebauer, and N. S. Sariciftci, "Current versus gate voltage hysteresis in organic field effect transistors," *Monatshefte fur Chemie*, vol. 140, no. 7, pp. 735–750, 2009.
[100] K.-H. Oh, "Investigation of ESD Performance in Advanced CMOS Technology," Stanford University, 2002.
[101] V. Koen, P. J. Roussel, G. Groeseneken, H. E. Maes, H. Gieser, C. Russ, P. Egger, X. Guggenmos, and F. G. Kuper, "Specifications Using a Fourth-Order Lumped Element Model," *Qual. Reliab. Eng. Int.*, vol. 10, no. June 1993, pp. 325–334, 1994.
[102] H. Gieser and M. Haunschild, "Very fast transmission line pulsing of integrated structures and the charged device model," *IEEE Trans. components, Packag. Manuf. Technol. Part C. Manuf.*, vol. 21, no. 4, pp. 278–285, 1998.
[103] A. Amerasekera, D. Charvana, and H. Gieser, "ESD in silicon integrated circuits," *John Wiley Son Ltd*, 1995.
[104] Y. Zhou, T. M. Khan, J. C. Liu, C. Fuentes-Hernandez, J. W. Shim, E. Najafabadi, J. P. Youngblood, R. J. Moon, and B. Kippelen, "Efficient recyclable organic solar cells on cellulose nanocrystal substrates with a conducting polymer top electrode deposited by film-transfer lamination," *Org. Electron. physics, Mater. Appl.*, vol. 15, no. 3, pp. 661–666, 2014.
[105] W. Liu, "Design, Characterization and Analysis of Electrostatic Discharge (ESD) Protection Solutions in Emerging and Modern Technologies," M.S. University of Central Florida, 2010.
[106] J. E. Vinson and J. J. Liou, "Electrostatic discharge in semiconductor devices: protection techniques," *Proc. IEEE*, vol. 88, no. 12, pp. 1878–1902, 2000.
[107] Ming-Dou Ker, Jeng-Jie Peng, and Hsin-Chin Jiang, "ESD test methods on integrated circuits: an overview," in *ICECS 2001. 8th IEEE International Conference on Electronics, Circuits and*

Systems (Cat. No.01EX483), vol. 2, pp. 1011–1014.
[108] W. Liu, J. J. Liou, K. Kuribara, K. Fukuda, T. Sekitani, T. Someya, J. Chung, Y. H. Jeong, Z. Wang, and C. L. Lin, "Study of organic thin-film transistors under electrostatic discharge stresses," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 967–969, 2011.
[109] T. J. Maloney, "Evaluating TLP Transients and HBM Waveforms," in *EOS/ESD Symposium 09*, 2009.
[110] D. Bonfert, G. Klink, H. Gieser, K. Bock, P. Svasta, and C. Ionescu, "Electrical stress on film resistive structures on flexible substrates," in *3rd Electronics System Integration Technology Conference ESTC*, 2010, pp. 1–6.
[111] W. Stadler, X. Guggenmos, P. Egger, H. Gieser, and C. Musshoff, "Does the ESD-failure current obtained by transmission-line pulsing always correlate to human body model tests?," *Microelectron. Reliab.*, vol. 38, no. 11, pp. 1773–1780, Nov. 1998.
[112] A. Z. H. Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang, and C. Zhang, "A Review on RF ESD Protection Design," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1304–1311, Jul. 2005.
[113] K. Bhatia, N. Jack, and E. Rosenbaum, "Layout Optimization of ESD Protection Diodes for High-Frequency I/Os," *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 3, pp. 465–475, Sep. 2009.
[114] J. J. Liou, W. Liu, K. Kuribara, K. Fukuda, T. Sekitani, T. Someya, and S. Luo, "Investigation of organic thin-film transistors for electrostatic discharge applications," *Proc. Int. Symp. Phys. Fail. Anal. Integr. Circuits, IPFA*, vol. 2, pp. 2–5, 2011.
[115] T. Lim, L. Santarelli, F. Cacialli, and H. Gieser, "Electrostatic discharge sensitivity investigation on organic field-effect thin film transistors," in *Conference Proceedings - 13th IEEE International NEW Circuits and Systems Conference, NEWCAS 2015*, 2015, pp. 8–11.
[116] L. Santarelli, T. Lim, G. M. Paternò, H. Wolf, H. Gieser, and F. Cacialli, "The Resilience of Poly(3-hexylthiophene-2,5-diyl) (P3HT) Field-Effect Transistors (FETs) with respect to Electrostatic Discharge (ESD) Effects," in *14th ESD Forum*, 2015.
[117] D. S. Sivia, *Elementary scattering theory : for X-ray and neutron users*. Oxford University Press, 2011.
[118] G. L. Squires, *Introduction to the theory of thermal neutron scattering*. Cambridge University Press, 2012.
[119] V. G. Sakai and A. Arbe, "Quasielastic neutron scattering in soft matter," *Curr. Opin. Colloid Interface Sci.*, vol. 14, no. 6, pp. 381–390, Dec. 2009.
[120] C. Andreani, A. Pietropaolo, A. Salsano, G. Gorini, M. Tardocchi, A. Paccagnella, S. Gerardin, C. D. Frost, S. Ansell, and S. P. Platt, "Facility for fast neutron irradiation tests of electronics at the ISIS spallation neutron source," *Appl. Phys. Lett.*, vol. 92, no. 11, p. 114101, Mar. 2008.
[121] J. Mayers, J. Tomkinson, T. Abdul-Redah, W. . Stirling, C. Andreani, R. Senesi, M. Nardone, D. Colognesi, and E. Degiorgi, "VESUVIO-the double difference inverse geometry spectrometer at ISIS," *Phys. B Condens. Matter*, vol. 350, no. 1–3, pp. E659–E662, Jul. 2004.
[122] M. J. Joung, C. A. Kim, S. Y. Kang, K.-H. Baek, G. H. Kim, S. D. Ahn, I. K. You, J. H. Ahn, and K. S. Suh, "The application of soluble and regioregular poly(3-hexylthiophene) for organic thin-film transistors," *Synth. Met.*, vol. 149, no. 1, pp. 73–77, Feb. 2005.
[123] S. A. Choulis, Y. Kim, J. Nelson, D. D. C. Bradley, M. Giles, M. Shkunov, and I. McCulloch, "High ambipolar and balanced carrier mobility in regioregular poly(3-hexylthiophene)," *Appl. Phys. Lett.*, vol. 85, no. 17, pp. 3890–3892, Oct. 2004.
[124] S. A. Choulis, J. Nelson, Y. Kim, D. Poplavskyy, T. Kreouzis, J. R. Durrant, and D. D. C. Bradley, "Investigation of transport properties in polymer/fullerene blends using time-of-flight photocurrent measurements," *Appl. Phys. Lett.*, vol. 83, no. 18, pp. 3812–3814, 2003.
[125] E. von Hauff, V. Dyakonov, and J. Parisi, "Study of field effect mobility in PCBM films and

P3HT:PCBM blends," *Sol. Energy Mater. Sol. Cells*, vol. 87, no. 1–4, pp. 149–156, May 2005.
[126] F. Cicoira and C. Santato, "Organic Light Emitting Field Effect Transistors: Advances and Perspectives," *Adv. Funct. Mater.*, vol. 17, no. 17, pp. 3421–3434, Nov. 2007.
[127] C. R. McNeill and N. C. Greenham, "Conjugated-Polymer Blends for Optoelectronics," *Adv. Mater.*, vol. 21, no. 38, pp. 3840–3850, Oct. 2009.
[128] Y. Zhang and P. W. M. Blom, "Electron and hole transport in poly(fluorene-benzothiadiazole)," *Appl. Phys. Lett.*, vol. 98, no. 14, p. 143504, Apr. 2011.
[129] M. Suh, J. Bailey, S. W. Kim, K. Kim, D.-J. Yun, Y. Jung, I. Hamilton, N. Chander, X. Wang, D. D. C. Bradley, D. Y. Jeon, and J.-S. Kim, "High-Efficiency Polymer LEDs with Fast Response Times Fabricated via Selection of Electron-Injecting Conjugated Polyelectrolyte Backbone Structure," *ACS Appl. Mater. Interfaces*, vol. 7, no. 48, pp. 26566–26571, Dec. 2015.
[130] J. Robertson, "High dielectric constant oxides," *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, Dec. 2004.
[131] R. Singh, "C. V. Raman and the Discovery of the Raman Effect," *Phys. Perspect.*, vol. 4, no. 4, pp. 399–420, Dec. 2002.
[132] S. Kasiouli, F. Di Stasio, S. O. McDonnell, C. P. Constantinides, H. L. Anderson, F. Cacialli, and S. C. Hayes, "Resonance Raman investigation of β-cyclodextrin-encapsulated π-conjugated polymers," *J. Phys. Chem. B*, vol. 117, no. 18, pp. 5737–5747, 2013.
[133] R. Stevenson, A. C. Arias, C. Ramsdale, J. D. Mackenzie, and D. Richards, "Raman microscopy determination of phase composition in polyfluorene composites," *Appl. Phys. Lett.*, vol. 79, no. 14, pp. 2178–2180, 2001.
[134] C. Kittel and H. Y. Fan, *Introduction to Solid State Physics*, vol. 25, no. 5. 1957.
[135] D. J. Gardiner, P. R. Graves, and H. J. Bowley, *Practical Raman spectroscopy*. Springer-Verlag, 1989.
[136] D. J. Gardiner, "Introduction to Raman Scattering," in *Practical Raman Spectroscopy*, Berlin, Heidelberg: Springer Berlin Heidelberg, 1989, pp. 1–12.
[137] W. C. Tsoi, D. T. James, J. S. Kim, P. G. Nicholson, C. E. Murphy, D. D. C. Bradley, J. Nelson, and J. S. Kim, "The nature of in-plane skeleton Raman modes of P3HT and their correlation to the degree of molecular order in P3HT:PCBM blend thin films," *J. Am. Chem. Soc.*, vol. 133, no. 25, pp. 9834–9843, 2011.
[138] R. Bedogni, A. Esposito, C. Andreani, R. Senesi, M. P. De Pascale, P. Picozza, A. Pietropaolo, G. Gorini, C. D. Frost, and S. Ansell, "Characterization of the neutron field at the ISIS-VESUVIO facility by means of a bonner sphere spectrometer," *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 612, no. 1, pp. 143–148, Dec. 2009.
[139] T. W. Armstrong and B. L. Colborn, "Predictions of secondary neutrons and their importance to radiation effects inside the International Space Station.," *Radiat. Meas.*, vol. 33, no. 3, pp. 229–34, Jun. 2001.
[140] G. Gruner, "Carbon nanotube films for transparent and plastic electronics," *J. Mater. Chem.*, vol. 16, no. 35, p. 3533, 2006.
[141] J. H. Borroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R. H. Friend, P. L. Burns, and A. B. Holmes, "Light-emitting diodes based on conjugated polymers," *Nature*, vol. 347, 1990.
[142] P. K. H. Ho, J.-S. Kim, J. H. Burroughes, H. Becker, S. F. Y. Li, T. M. Brown, F. Cacialli, and R. H. Friend, "Molecular-scale interface engineering for polymer light-emitting diodes," *Nature*, vol. 404, no. 6777, pp. 481–484, 2000.
[143] J. Ge, L. Sun, F.-R. Zhang, Y. Zhang, L.-A. Shi, H.-Y. Zhao, H.-W. Zhu, H.-L. Jiang, and S.-H. Yu, "Stretchable Electronics: A Stretchable Electronic Fabric Artificial Skin with Pressure-, Lateral Strain-, and Flexion-Sensitive Properties (Adv. Mater. 4/2016)," *Adv. Mater.*, vol. 28, no. 4,

pp. 783–783, Jan. 2016.
[144] T. Someya, S. Iba, Y. Kato, T. Sekitani, Y. Noguchi, Y. Murase, H. Kawaguchi, and T. Sakurai, “A large-area, flexible, and lightweight sheet image scanner integrated with organic field-effect transistors and organic photodiodes,” *IEDM Tech. Dig. IEEE Int. Electron Devices Meet. 2004.*, pp. 365–368, 2004.
[145] M. S. White, M. Kaltenbrunner, E. D. Głowacki, K. Gutnichenko, G. Kettlgruber, I. Graz, S. Aazou, C. Ulbricht, D. A. M. Egbe, M. C. Miron, Z. Major, M. C. Scharber, T. Sekitani, T. Someya, S. Bauer, and N. S. Sariciftci, “Ultrathin , highly flexible and stretchable PLEDs,” *Nat. Photonics*, no. July, 2013.
[146] G. Kettlgruber, M. Kaltenbrunner, C. M. Siket, R. Moser, I. M. Graz, R. Schwödiauer, and S. Bauer, “Intrinsically stretchable and rechargeable batteries for self-powered stretchable electronics,” *J. Mater. Chem. A*, vol. 1, no. 18, pp. 5505–5508, 2013.
[147] M. L. Hammock, A. Chortos, B. C. K. Tee, J. B. H. Tok, and Z. Bao, “25th anniversary article: The evolution of electronic skin (E-Skin): A brief history, design considerations, and recent progress,” *Adv. Mater.*, vol. 25, no. 42, pp. 5997–6038, 2013.
[148] H.-S. Kim, C.-R. Lee, J.-H. Im, K.-B. Lee, T. Moehl, A. Marchioro, S.-J. Moon, R. Humphry-Baker, J.-H. Yum, J. E. Moser, M. Grätzel, and N.-G. Park, “Lead iodide perovskite sensitized all-solid-state submicron thin film mesoscopic solar cell with efficiency exceeding 9%.,” *Sci. Rep.*, vol. 2, no. 7436, p. 591, 2012.
[149] Z. Wu, W. Ren, L. Gao, J. Zhao, Z. Chen, B. Liu, D. Tang, B. Yu, C. Jiang, and H. Cheng, “Synthesis of Graphene Sheets with High Electrical Conductivity and Good Discharge Exfoliation,” vol. 3, no. 2, pp. 411–417, 2009.
[150] W. Wang, M. T. Winkler, O. Gunawan, T. Gokmen, T. K. Todorov, Y. Zhu, and D. B. Mitzi, “Device Characteristics of CZTSSe Thin-Film Solar Cells with 12.6% Efficiency,” *Adv. Energy Mater.*, vol. 4, no. 7, p. n/a-n/a, May 2014.
[151] L. Yang, T. Zhang, H. Zhou, S. C. Price, B. J. Wiley, and W. You, “Solution-processed flexible polymer solar cells with silver nanowire electrodes.,” *ACS Appl. Mater. Interfaces*, vol. 3, no. 10, pp. 4075–84, 2011.
[152] Z. Chen, B. Cotterell, W. Wang, E. Guenther, and S. Chua, “A mechanical assessment of flexible optoelectronic devices,” *Thin Solid Films*, pp. 202–206, 2001.
[153] J. He, R. G. Nuzzo, and J. A. Rogers, “Inorganic Materials and Assembly Techniques for Flexible and Stretchable Electronics,” *Proc. IEEE*, vol. 103, no. 4, pp. 619–632, 2015.
[154] Z. Chen, B. Cotterell, and W. Wang, “The fracture of brittle thin films on compliant substrates in flexible displays,” *Eng. Fract. Mech.*, vol. 69, pp. 597–603, 2002.
[155] D. Bonfert, D. Hemmetzberger, I. Bose, G. Klink, K. Bock, P. Svasta, and C. Ionescu, “Electrical stress on intrinsically conductive polymer layer,” *Proc. Int. Spring Semin. Electron. Technol.*, pp. 270–275, 2012.
[156] D. Bonfert and C. Ionescu, “Pulsed Stress Behavior of PEDOT : PSS Thin Films,” in *SIITME2009 - 15th International Symposium for Design and Technology of Electronics Packages*, 2009, pp. 75–80.
[157] B. Park, C. H. Park, Y. Yim, and J. Park, “Electrical annealing for flexible organic light-emitting diodes having poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) anodes,” *J. Appl. Phys.*, vol. 108, no. 8, p. 84508, 2010.
[158] T.-W. Lee and O. O. Park, “Effect of electrical annealing on the luminous efficiency of thermally annealed polymer light-emitting diodes,” *Appl. Phys. Lett.*, vol. 77, no. 21, p. 3334, 2000.
[159] S. H. Voldman, “The state of the art of electrostatic discharge protection: physics, technology, circuits, design, simulation and scaling,” *Proc. 1998 Bipolar/BiCMOS Circuits Technol. Meet.*

(Cat. No.98CH36198), vol. 34, no. 9, pp. 19–30, 1999.
[160] O. Breitenstein, J. Bauer, K. Bothe, W. Kwapil, D. Lausch, U. Rau, J. Schmidt, M. Schneemann, M. C. Schubert, J.-M. Wagner, and W. Warta, "Understanding junction breakdown in multicrystalline solar cells," *J. Appl. Phys.*, vol. 109, no. 7, p. 71101, 2011.
[161] X. Jiang, R. Österbacka, O. Korovyanko, C. P. An, B. Horovitz, R. A. J. Janssen, and Z. Valy Vardeny, "Spectroscopic Studies of Photoexcitations in Regioregular and Regiorandom Polythiophene Films," *Adv. Funct. Mater.*, vol. 12, no. 9, 2002.
[162] G. Tregnago, M. Wykes, G. M. Paternò, D. Beljonne, and F. Cacialli, "Low-Temperature Photoluminescence Spectroscopy of Solvent-Free PCBM Single-Crystals," *J. Phys. Chem. C*, vol. 119, no. 21, pp. 11846–11851, 2015.
[163] S. Cook, H. Ohkita, Y. Kim, J. J. Benson-Smith, D. D. C. Bradley, and J. R. Durrant, "A photophysical study of PCBM thin films," *Chem. Phys. Lett.*, vol. 445, no. 4–6, pp. 276–280, 2007.
[164] R. Ozgun, B. J. Jung, B. M. Dhar, H. E. Katz, and A. G. Andreou, "Silicon-on-insulator (SOI) integration for organic field effect transistor (OFET) based circuits," *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 2253–2256, 2011.
[165] C. M. Osburn and E. J. Weitzman, "Dielectric Breakdown in Silicon Dioxide Films on Silicon," *J. Electrochem. Soc.*, vol. 119, no. 5, p. 603, 1972.
[166] M. Baibarac, M. Lapkowski, A. Pron, S. Lefrant, and I. Baltog, "SERS spectra of poly(3-hexylthiophene) in oxidized and unoxidized states," *J. Raman Spectrosc.*, vol. 29, no. 9, pp. 825–832, 1998.
[167] T. N. M. Cervantes, D. C. Bento, E. C. R. Maia, D. A. M. Zaia, E. Laureto, M. A. T. da Silva, G. J. Moore, and H. de Santana, "In situ and ex situ spectroscopic study of poly(3-hexylthiophene) electrochemically synthesized," *J. Mater. Sci. Mater. Electron.*, vol. 23, no. 10, pp. 1916–1921, Oct. 2012.
[168] D. C. Bento, E. A. da Silva, C. de Almeida Olivati, G. Louarn, and H. de Santana, "Characterization of the interaction between P3ATs with PCBM on ITO using in situ Raman spectroscopy and electrochemical impedance spectroscopy," *J. Mater. Sci. Mater. Electron.*, vol. 26, no. 10, pp. 7844–7852, Oct. 2015.
[169] J. Yamamoto and Y. Furukawa, "Electronic and Vibrational Spectra of Positive Polarons and Bipolarons in Regioregular Poly(3-hexylthiophene) Doped with Ferric Chloride," *J. Phys. Chem. B*, vol. 119, no. 13, pp. 4788–4794, Apr. 2015.
[170] S. Sweetnam, K. Vandewal, E. Cho, C. Risko, V. Coropceanu, A. Salleo, J.-L. Breas, and M. D. Mcgehee, "Characterizing the Polymer:Fullerene Intermolecular Interactions," *Chem. Mater.*, vol. 28, pp. 1446–1452, 2016.
[171] C. Francis, D. Fazzi, S. B. Grimm, F. Paulus, S. Beck, S. Hillebrandt, A. Pucci, J. Zaumseil, S. R. Marder, P. Wasserscheid, J. Zaumseil, H. Tanaka, S. -i. Kuroda, H. Sirringhaus, G. Seifert, B. Voit, R. Di Pietro, and A. Kiriy, "Raman spectroscopy and microscopy of electrochemically and chemically doped high-mobility semiconducting polymers," *J. Mater. Chem. C*, vol. 83, pp. 5539–5541, 2017.
[172] L.-H. Zhao, R.-Q. Png, J.-M. Zhuo, L.-Y. Wong, J.-C. Tang, Y.-S. Su, and L.-L. Chua, "Role of Borderline Solvents to Induce Pronounced Extended-Chain Lamellar Order in π-Stackable Polymers," *Macromolecules*, vol. 44, no. 24, pp. 9692–9702, Dec. 2011.
[173] I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner, W. Zhang, M. L. Chabinyc, R. J. Kline, M. D. McGehee, and M. F. Toney, "Liquid-crystalline semiconducting polymers with high charge-carrier mobility," *Nat. Mater.*, vol. 5, no. 4, pp. 328–333, Apr. 2006.
[174] A. C. Mayer, M. F. Toney, S. R. Scully, J. Rivnay, C. J. Brabec, M. Scharber, M. Koppe, M.

Heeney, I. McCulloch, and M. D. McGehee, “Bimolecular Crystals of Fullerenes in Conjugated Polymers and the Implications of Molecular Mixing for Solar Cells,” *Adv. Funct. Mater.*, vol. 19, no. 8, pp. 1173–1179, Apr. 2009.

[175] O. Fenwick, S. Fusco, T. N. Baig, F. Di Stasio, T. T. Steckler, P. Henriksson, C. Flechon, M. R. Andersson, and F. Cacialli, “Efficient red electroluminescence from diketopyrrolopyrrole copolymerised with a polyfluorene,” *APL Mater.*, vol. 1, no. 3, 2013.

[176] A. Charas, H. Alves, L. Alcácer, and J. Morgado, “Use of cross-linkable polyfluorene in the fabrication of multilayer polyfluorene-based light-emitting diodes with improved efficiency,” *Appl. Phys. Lett.*, vol. 89, no. 14, p. 143519, Oct. 2006.

[177] P. E. Burrows, Z. Shen, V. Bulovic, D. M. McCarty, S. R. Forrest, J. A. Cronin, and M. E. Thompson, “Relationship between electroluminescence and current transport in organic heterojunction light-emitting devices,” *J. Appl. Phys.*, vol. 79, Jun. 1996.

[178] T. Okachi, T. Nagase, T. Kobayashi, and H. Naito, “Determination of Charge-Carrier Mobility in Organic Light-Emitting Diodes by Impedance Spectroscopy in Presence of Localized States,” *Jpn. J. Appl. Phys.*, vol. 47, no. 12, pp. 8965–8972, Dec. 2008.

[179] J.-H. Lee, J. Lee, Y. H. Kim, C. Yun, B. Lüssem, and K. Leo, “Effect of trap states on the electrical doping of organic semiconductors,” *Org. Electron.*, vol. 15, no. 1, pp. 16–21, Jan. 2014.

[180] R. F. Pease and S. Y. Chou, “Lithography and other patterning techniques for future electronics,” *Proc. IEEE*, vol. 96, no. 2, pp. 248–270, 2008.

[181] S. Cherian, H. Spangenberg, and R. Caspary, “Integrating polymer optical fibers in civil aircraft: Enviromental requirements and challenges,” in *2010 Avionics, Fiber-Optics and Photonics Technology Conference*, 2010, pp. 11–12.

[182] T. Gu, Y. Lu, J. Q. Zhong, R. Brinkley, G. Xu, W. den Boer, and S. V. Thomsen, “Low-reflection high-transmission wide-viewing-angle TFT-LCDs for avionics applications,” *SPIE*, pp. 41–48, Aug. 1998.

[183] R. L. Crabb and F. C. Treble, “Thin Silicon Solar Cells for Large Flexible Arrays,” *Nature*, 1967.

[184] T. Straume, C. J. Mertens, T. C. Lusby, B. Gersey, W. K. Tobiska, R. B. Norman, G. P. Gronoff, and A. Hands, “Ground-based evaluation of dosimeters for NASA high-altitude balloon flight,” *Sp. Weather*, vol. 14, no. 11, pp. 1011–1025, Nov. 2016.

[185] T. A. Bergstralh and C. A. Schroeder, “A Search for Cosmic-Ray Diurnal Effects at Balloon Altitudes,” *Phys. Rev.*, vol. 81, no. 2, pp. 244–247, Jan. 1951.

[186] F. Moupfouma, “Electrostatic Discharge Phenomenon: A Potential Threat to Aircraft Safety,” *SAE Tech. Pap.*, vol. 1, p. 3833, Sep. 2007.

[187] T.-J. Ha, D. Sparrowe, and A. Dodabalapur, “Device architectures for improved amorphous polymer semiconductor thin-film transistors,” *Org. Electron.*, vol. 12, no. 11, pp. 1846–1851, Nov. 2011.

[188] P. Pingel, R. Schwarzl, and D. Neher, “Effect of molecular p-doping on hole density and mobility in poly(3-hexylthiophene),” *Appl. Phys. Lett.*, vol. 100, no. 14, p. 143303, Apr. 2012.

[189] V. F. Sears, “Neutron scattering lengths and cross sections,” *Neutron News*, vol. 3, no. 3, pp. 26–37, Jan. 1992.

[190] J. A. Horak and T. H. Blewitt, “Fast neutron irradiation induced resistivity in metals,” *Phys. Status Solidi*, vol. 9, no. 2, pp. 721–730, Feb. 1972.

[191] V. Nagesh, J. W. Farmer, R. F. Davis, and H. S. Kong, “Defects in neutron irradiated SiC,” *Appl. Phys. Lett.*, vol. 50, no. 17, pp. 1138–1140, Apr. 1987.

[192] W. Dong, T. Fei, A. Palma-Cando, and U. Scherf, “Aggregation induced emission and amplified explosive detection of tetraphenylethylene-substituted polycarbazoles,” *Polym. Chem.*, vol. 5, no. 13, p. 4048, 2014.

[193] B. Fraboni, A. Matteucci, A. Cavallini, E. Orgiu, and A. Bonfiglio, “Photocurrent studies of

stress and aging in pentacene thin film transistors," *Appl. Phys. Lett.*, vol. 89, no. 22, pp. 3–5, 2006.
[194] H. J. Snaith, "Perovskites : The Emergence of a New Era for Low-Cost , High-," *J. Phys. Chem. Lett*, vol. 4, p. 3623−3630, 2013.
[195] E. G. Stassinopoulos and J. P. Raymond, "The space radiation environment for electronics," *Proc. IEEE*, vol. 76, no. 11, pp. 1423–1442, 1988.